IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al. Defendants.	)	Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF) CONSOLIDATED CASES

APPENDIX IN SUPPORT OF DEFENDANT CHI MEI OPTOELECTRONICS' PROPOSED CLAIM CONSTRUCTIONS

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Dated: August 11, 2008

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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EXHIBIT A-2

Moving back to the lab, the next step will be to understand in molecular detail where survival pathways and chemotherapy agents intersect. ■

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Semiconductor physics

Quick-set thin films

Mercouri G. Kanatzidis

Transistors that have active components based on thin films, rather than silicon, are attractive for many applications. The latest thin-film fabrication technique has the potential for industrial-scale production.

The original working transistor, invented at Bell Labs in the 1940s, was based on semiconducting germanium and had a junction (sandwich) configuration. But by the 1960s, this design had given way to the simpler field-effect transistor — in particular, the silicon-based MOSFET (for metal-oxide-semiconductor field-effect transistor). A typical computer processor today contains around 42 million such transistors, and demand for ever-faster computers is only increasing. As a result, the market is pushing for a downsizing of transistor technology.

However, certain applications (such as flat-panel displays) require larger-area transistors than can normally be created using silicon-based devices. Thin-film semiconductors have been explored as an alternative, although with limited success. But now it seems that the large-scale, low-cost fabrication of such devices is a step closer: on page 299 of this issue, Mitzi *et al.*[1] describe a chemical-deposition method for producing uniform films of the chalcogenides SnS_2 or $SnSe_2$ for use in thin-film transistors (TFTs). The resulting TFTs support large current densities (more than 10^5 A cm^{-2}), and mobilities greater than 10 cm^2 V^{-1} s^{-1} — almost ten times larger than achieved for semiconducting films formed using the spin-coating technique (in which a solution on a substrate is spun rapidly, causing the film to spread outwards).

In a TFT, the thin film (usually silicon) is the active current-carrying layer (Fig. 1). The film sits on a substrate, which is usually glass owing to its low cost, high optical transparency and compatibility with conventional semiconductor processing technology. Recently, however, plastic has emerged as a viable challenger because of its additional flexibility, although the development of TFT technology for use with plastic substrates is still in its infancy.

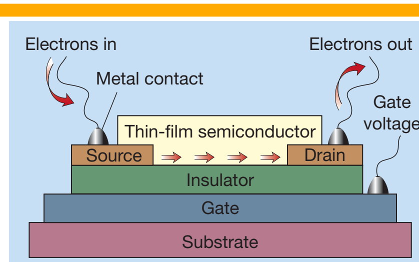

Figure 1 **Cross-section of a thin-film transistor. A voltage applied at the gate controls the flow of electrons (resistance) from the source to the drain; a positive gate voltage attracts electrons to the bottom surface of the semiconductor layer and creates a conduction channel. When a voltage difference is applied between the two connector wires, electrons enter at one end (the source) and exit at the other (the drain), resulting in a current along the channel. Mitzi *et al.*[1] have now come up with a chemical-deposition method that produces uniform films of the chalcogenide $SnSe_2$ for use in thin-film transistors.**

Transistors for high-performance display applications should have high electron mobilities, low leakage currents and low threshold voltages. But processing temperatures must also be low (below 150 °C) if the transistors are to be compatible with low-cost plastic substrate materials. So the emphasis in developing large-scale TFTs has been on low-temperature deposition and the exploration of materials other than amorphous silicon. Approaches include vacuum deposition[2] (suitable for growing ultrathin organic films and multilayer structures), solution-deposition technologies[3] (suitable for inorganic materials), and many others[4]. But these are generally not high-throughput processes. Although spin-coated semiconductor films have suffered from low mobilities[5–7], this technique shows much promise.

The attraction of using inorganic semiconductors lies in their stability, thermal robustness and high mobilities. The metal chalcogenides, for example, are excellent candidates for use in TFT technologies. They form a large class of compounds that are composed of one or more metals plus one of the chalcogen atoms such as sulphur, selenium or tellurium. Moreover, the energy required to delocalize a charge carrier (the energy gap)[8] in these materials is suitable for room-temperature devices, and can be further tuned for a given application[9].

Mitzi *et al.*[1] describe a means of creating chalcogenide active layers for TFTs through spin coating. Their continuous, uniform, ultrathin semiconducting films are only a few unit cells thick. The key to the fabrication chemistry is hydrazine (N_2H_4), which Mitzi *et al.* use as a solvent. When metal and chalcogens dissolve in hydrazine, they form chalcogenometallate solutions containing anions such as $[Sn_2S_6]^{4-}$, as well as hydrazinium cations $(N_2H_5)^+$. These solutions can be used as precursors for spin-coating thin films of the salt $(N_2H_5)_4[Sn_2S_6]$, which then decompose to the binary metal chalcogenide at low temperature. The advantage of having hydrazinium cations, and not some other organic cations[10], is that they readily and cleanly react with the counterion of $[Sn_2S_6]^{4-}$ to give continuous, crystalline semiconducting films as thin as 5 nanometres.

It is this simple chemistry that not only makes the work of Mitzi *et al.*[1] attractive, but probably technologically significant as well. Thin films produced by deposition from solution have so far been moderately successful in terms of their mobilities[11–13], but the techniques are generally not suitable for high throughput. This hydrazine-based process can be applied more generally, and the hydrazinium salts need not be isolated first — they can be made *in situ*. If the process can be optimized and scaled up, thin films for high-performance channel layers in TFTs could be fabricated with all the processing performed at 300 °C. In principle, depending on the specific metal chalcogenide involved, the films could be made at even lower temperatures.

However, the current processing temperature is too high for many applications (such as those using plastic substrates), and the mobilities achieved, although much higher than reported for other techniques, may not yet be adequate for many devices. Furthermore, the source and gate voltages of the TFTs are higher than those of typical silicon-based devices, while little is known about the yield and reproducibility of these devices. And the substrate is still silicon, not glass or plastic, which will limit the fabrication of TFTs on large-area, low-cost substrates.

So there are several factors to be considered before a new generation of optoelectronic devices based on this deposition

technology could gain a foothold, including the long-term operational and environmental stability of the devices. But, given the relative youth of this technology, and the exciting and rapid advances anticipated using chalcogenide thin films, the goal does not seem unattainable. Continued work in this area is likely to contribute to our understanding and exploitation of these exciting materials well into the next century. ■

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Cancer

Dangerous liaisons

Allan Balmain and Rosemary J. Akhurst

The cells of multicellular organisms are highly communicative and so can strongly influence one another's behaviour. One line of communication is particularly important in keeping cell growth in check.

A single cell destined to become a tissue or an organism can't go it alone in its rise to such dizzy heights. Communication, in the form of direct contacts between cells, interactions between cells and their surroundings, or the transmission of biochemical signals, is essential. Unravelling these networks of communication has provided gainful employment for biologists, geneticists and mathematicians in their quest to understand how the body forms[1]. But now cancer biologists are being drawn into a similar web of interactions between cells targeted to become tumours (usually epithelial cells) and their neighbours (stromal fibroblasts). A network of signals operates in tumours. As they describe in *Science*, Bhowmick *et al.*[2] have identified one signalling pathway — regulated by transforming growth factor β (TGF-β) — that is an important mediator of the stromal–epithelial interactions modulating the growth of solid tumours.

It has been known[3] for some years that normal stromal cells inhibit tumour growth whereas tumour-associated stromal cells stimulate it (Fig. 1). In their study, Bhowmick *et al.*[2] deleted the receptor for TGF-β — the TGF-β type II receptor — specifically in stromal cells of otherwise normal mice. This 'selective knockout' avoided killing the animals by deleting the TGF-β type II receptor in every cell type, completely inhibiting signalling through this pathway in the stroma of several tissues. Surprisingly, although the deletion occurs in the skin, oesophagus, kidney, liver and lung, mice were born normally, and these tissues showed no observable adverse effects.

Not everything, however, escaped unscathed. Prostate tissue underwent increased stromal-cell division, growing excessively by the time the animals were three weeks old. This, in turn, stimulated the epithelial cells of the prostate to divide and form lesions that resembled prostatic intraepithelial neoplasia, a probable forerunner of prostate cancer. The stromal-cell population in the animals' forestomach also proliferated more rapidly, in this case spurring the expansion of the epithelial population so that an invasive form of cancer occurred that killed the mice by the time they were seven weeks old. So not only does abrogation of TGF-β signalling in the stromal fibroblasts cause them to proliferate, but the ensuing perturbed communication with the epithelial cells causes dysregulated cell division, indirectly leading to cancerous growth.

What causes this? Perhaps the stromal cells that cannot respond to TGF-β instead release other factors, or greater amounts of certain factors than do normal stromal cells? Bhowmick *et al.*[2] suggest that it might be due to another growth factor, hepatocyte growth factor (HGF), acting through its receptor c-Met (Fig. 1). The HGF–c-Met regulatory system is important in proliferation, cell migration and metastasis — the movement of cancer cells to other parts of the body to establish more tumours[4]. Impressively, fibroblasts from both the forestomach and prostate tissues of the knockout mice secreted at least three times as much HGF as their normal counterparts, and c-Met was simultaneously activated in the proliferating epithelial cells of the forestomach tumours.

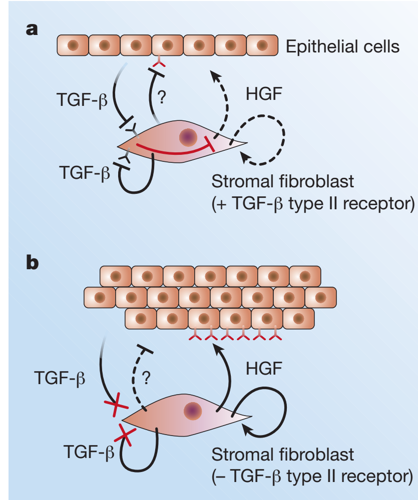

Figure 1 **Cellular relationships.** a, **Normal communications between epithelial cells and their fibroblast neighbours. Both epithelial cells and fibroblasts secrete transforming growth factor β (TGF-β), which suppresses growth. Stromal fibroblasts might also secrete other factors that inhibit epithelial-cell growth (denoted by ?). A small amount of hepatocyte growth factor (HGF; its receptor is c-Met) secreted by the stroma inhibits stromal-cell growth and also that of epithelial cells.** b, **Perturbed signalling in the absence of the receptor for TGF-β, the TGF-β type II receptor. Inhibition of TGF-β signalling in stromal cells prevents growth-inhibitory responses to TGF-β and stimulates the stroma to release higher levels of HGF, a positive growth and metastatic factor. The production of other growth-inhibitory factors (?) might be reduced in response to inhibition of TGF-β signalling. TGF-β receptors are shown in black, c-Met receptors in red.**

These data are consistent with previous reports that TGF-β normally inhibits HGF synthesis in stromal cells[5]. But they don't reflect the situation in advanced skin cancer, in which tumour-derived TGF-β induces adjacent stromal cells to produce HGF[6].

The study by Bhowmick and colleagues has uncovered insights into cellular liaisons within tissues that should benefit cancer researchers and developmental biologists alike. But several issues raised by the findings must first be resolved. The cells of most solid tumours secrete large amounts of TGF-β, but are insensitive to its growth-inhibitory effects. This means either that components of this signalling pathway have mutated or, as is more common, that the growth response has been reduced while the ability to migrate, invade and metastasize in response to TGF-β is retained. How, then, do stromal cells normally escape the growth-inhibitory effects of overexpressed TGF-β and become willing partners in fostering epithelial tumour progression? Possible answers are genetic changes, or changes in gene expression that occur without altering the DNA sequence.

EXHIBIT A-3

United States Patent [19] [11] **4,332,075**

Ota et al. [45] **Jun. 1, 1982**

[54] **METHOD OF PRODUCING THIN FILM TRANSISTOR ARRAY**

[75] Inventors: **Isao Ota,** Osaka; **Haruhiro Shirazawa,** Daito; **Toshio Tatsumichi,** Ando; **Hiroshi Kawarada,** Hirakata; **Tetsuro Ohtsuka,** Takatsuki; all of Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.,** Osaka, Japan

[21] Appl. No.: **41,507**

[22] Filed: **May 22, 1979**

[30] **Foreign Application Priority Data**

May 26, 1978 [JP] Japan 53-63598

[51] **Int. Cl.**^{3} **H01L 21/04;** H01L 21/12

[52] **U.S. Cl.** **29/571;** 29/572; 29/578; 29/591; 357/4

[58] **Field of Search** 29/572, 571, 591, 578; 357/4

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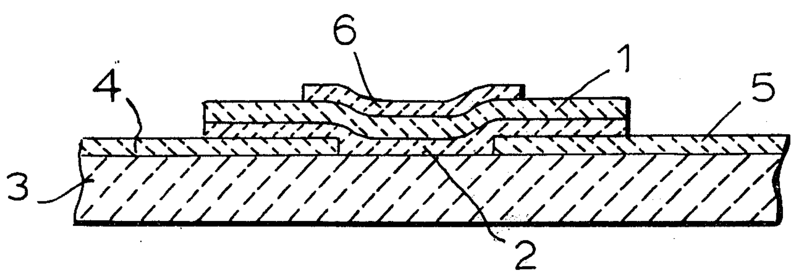
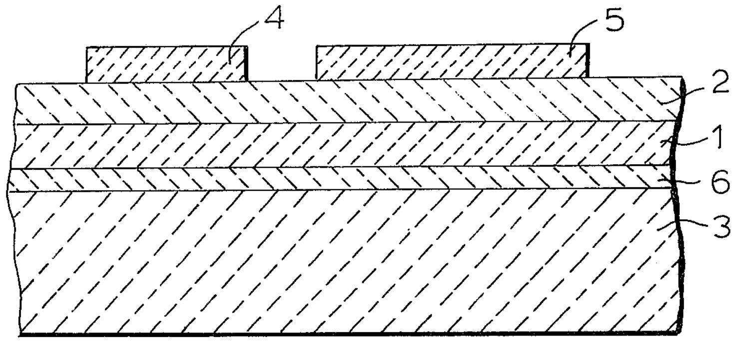
Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—Wenderoth, Lind & Ponack

[57] **ABSTRACT**

A method of producing thin film transistor arrays and having at least 7 steps including: a first step of forming a first electrode layer uniformly over an insulating substrate; a second step of forming electrodes, such as drain and source electrodes and bus bars with a desired pattern by photoetching the first electrode; a third step of forming a uniform semiconducting layer on the surface of the substrate having the patterned electrodes; a fourth step of successively forming a uniform insulating layer over the uniformly deposited semiconducting layer while keeping the array in a vacuum; a fifth step of photoetching the uniformly deposited insulating layer into a desired pattern; a sixth step of photoetching the uniform semiconducting layer into the same pattern as the patterned insulating layer; a seventh step of forming a second electrode uniformly over the surface having the patterned electrodes and insulating layer; and an eighth step of photoetching the uniformly deposited second electrode into a desired pattern.

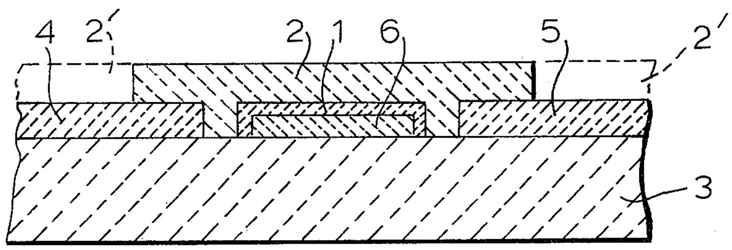
10 Claims, 7 Drawing Figures





(PRIOR ART)

FIG. 1



(PRIOR ART)

FIG. 2

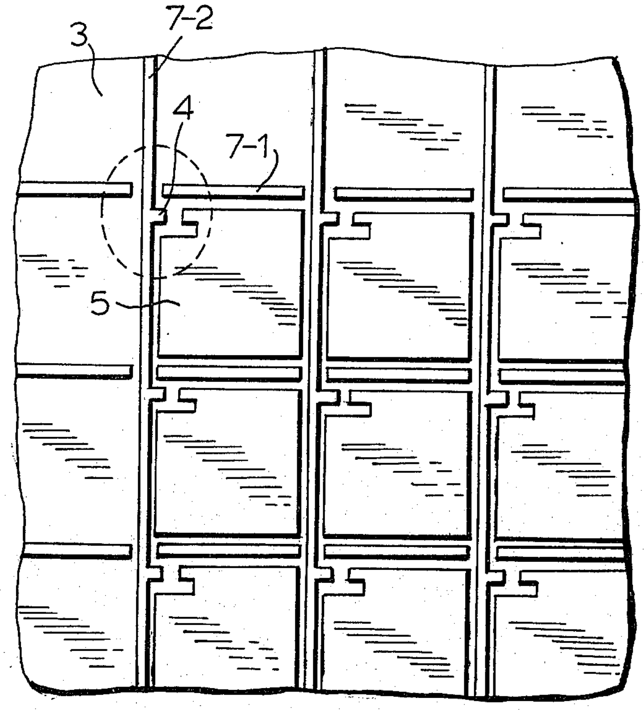


FIG. 3

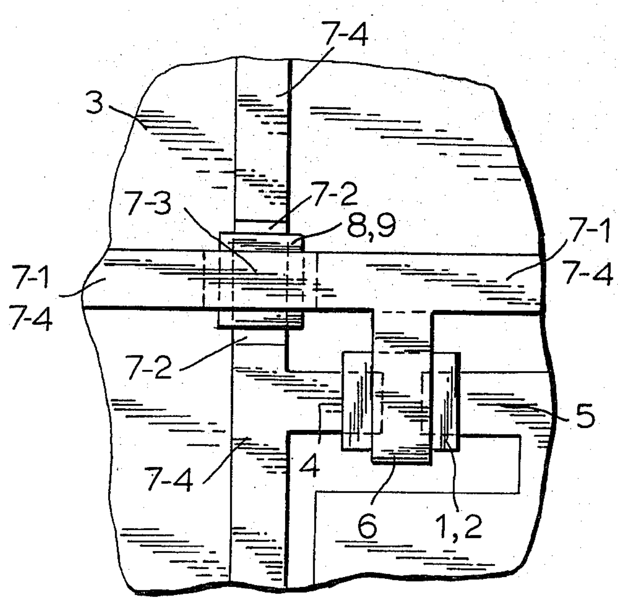


FIG. 4

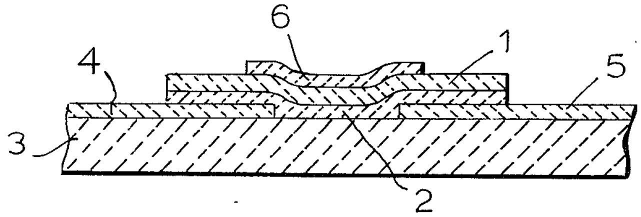


FIG.5

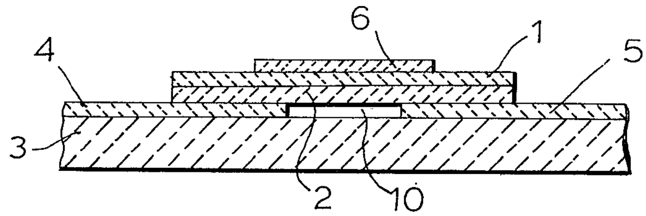


FIG.6

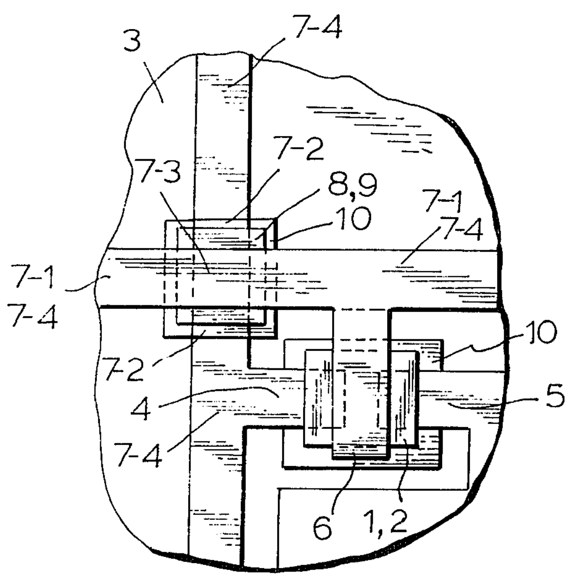


FIG.7

METHOD OF PRODUCING THIN FILM TRANSISTOR ARRAY

BACKGROUND OF THE INVENTION

This invention relates to a method of producing a thin film transistor (TFT) array.

Thin film transistors are known to be field effect transistors in which the conductivity of the semiconductor fabricated between the source electrode and the drain electrode is controlled by a voltage applied to the third electrode (gate electrode) formed on the gate insulator in contact with the semiconductor.

The thin film transistor has been studied for its application to image sensors or display panels because of the ease of fabricating a switching array over a large area at a low material cost. For example, a display panel having a thin film transistor at each picture element can be greatly improved in its performance. There are, at present, a lot of display media devices such as gas plasma, electroluminescence, fluorescent displays activated by a low voltage electron beam, liquid crystal, electrochromic, electrophoretic and so on. In order to have an excellent contrast on the matrix display panel utilizing these display media devices, it is essential that the display medium have a sharp threshold in the voltage-brightness characteristics. However, some of the display media described above lack this sharpness in the threshold and are not suitable for a matrix display with many picture elements. Furthermore, even the matrix display panel with sharp threshold characteristics suffers from the decrease in brightness or response speed due to the decrease in the duty ratio for activation as the picture elements increase. A thin film transistor switching element, and, if necessary, a storage capacitor at each picture element, thus serve to improve the contrast ratio, the brightness and the response speed in the matrix display panel with a large number of picture elements.

Conventional methods of producing thin film transistor arrays are reviewed, for example, in Physics of Thin Films, Vol. 2, pp. 147–190, 1964, by P. K. Weimer, Academy Press, and Proceedings of the Society for Information Display, Vol. 17, pp. 39–55, 1976, by T. B. Brody. In these conventional methods, electrodes, semiconductors and gate insulators with desired patterns are formed on an insulating substrate by vacuum deposition through a metal mask with a desired aperture in contact with the surface of the substrate. The conventional method in which materials forming the electrodes, semiconductors and gate insulators are successively deposited on each other under high vacuum by one pumpdown has advantages in that a clean layer without contamination can be obtained using fewer production steps. However, it has some disadvantages in that it is difficult to obtain an evaporation metal mask with high precision and no defects, and in that high cost equipment is necessary for the successive exchanges of metal masks or the precise adjustment of the relative position of the two metal masks.

Furthermore, a thin metal mask is essential for the fabrication of a thin film transistor array of high density, and it becomes more difficult to accomplish a uniform contact between a thin metal mask and the substrate due to a decrease in a mechanical strength of the metal mask.

Thus, in the conventional methods, integration density of the array and the precision in dimension and position of the fabricated thin film transistor are seriously incompatible to each other.

A further disadvantage in the conventional method is the problem in the mis-registration of deposited layers caused by the difference between the thermal expansion coefficients of the substrate and the metal mask. The thermal expansion coefficients of glass substrates per degree centigrade are between about 3×10^{-6} (Pyrex glass) and about 9×10^{-6} (soda glass). On the other hand, those of metal masks are, e.g., (1 to 2)$\times10^{-6}$ (invar), 6×10^{-6} (kovar), 16.4×10^{-6} (stainless steel: 18Cr, 8Ni). The difference of 1×10^{-6}/°C. in the thermal expansion coefficient between the substrate and the metal mask results in a misregistration of about 23 μm under the temperature of 250° C. in a dimension which is 100 mm at room temperature.

It is quite difficult to select a combination of the substrate and the metal mask with a difference in their thermal expansion coefficients less than 1×10^{-6}/°C., and at the same time the mis-registration of about 23 μm is an unacceptable amount. As described above, it is hopeless to fabricate, by the conventional method based on the use of metal masks, an array of large size with an integration density more than about 50 elements/inch.

A method of fabricating a thin film transistor array without using a metal mask is described, for example, in Proceedings of the SID, Vol. 14, No. 4, 1973 or in Philips Technical Review, Vol. 27, 1966.

According to these conventional methods, electrodes of source, drain or gate are formed by photolithography method. The thin film transistor according to the former one of the above-noted conventional methods has, as shown in FIG. **1**, features a structure wherein a gate insulating layer **1** and semiconducting layer **2** are deposited almost uniformly on the surface of the substrate **3**, without being patterned. On the other hand, the latter one of the above-noted conventional methods discloses the TFT structure as shown in FIG. **2** in which electrodes of source, drain and gate, **4**, **5**, **6**, respectively, are formed on the same surface of the substrate **3**, and a gate insulator **1** which is formed by an anodic oxidation method covers only the gate electrode **6**.

The present inventors have tried these conventional methods based on the use of metal masks or photolithography techniques in order to fabricate a TFT array with a high density, and have found that the metal mask method surfaces from a great difficulty when used for the purpose of fabricating a TFT array of high density, as already described before. On the other hand, as apparent from FIGS. **1** and **2**, those TFT's have the same feature that the semiconducting layer **2** is formed on the upper surface of the insulating layer **1** when viewed from the side of the substrate **3**.

The display panel combined with the TFT array usually uses, as display medium, an electroluminescence layer, a liquid crystal layer or a electrophoretic suspension layer. Such a display medium is usually sandwiched between the surface of the substrate with the TFT array and the common electrode. Therefore, the display medium is directly in contact with the surface of the semiconducting layer of the TFT. In order to avoid the deterioration in the characteristics of the display medium and/or the TFT's due to the electrochemical interaction between them, the semiconducting layer must be protected by an inert insulating layer. Since the protection layer must not cover the drain electrode which is electrically connected to the display medium,

the step of depositing an inert protection layer with a specific pattern becomes inevitable. Furthermore, the disadvantage in the structure as shown in FIG. **1** lies in that the semiconducting layer **2** is apt to deteriorate in its characteristics due to the direct contact with the solvent when etching the semiconducting layer into a desired pattern, and furthermore, the dissolving peeling or contamination of the semiconducting layer often arises.

The TFT structure as shown in FIG. **2** has a disadvantage that it is necessary to remove the portions **2'**, as shown in FIG. **2**, of the semiconducting layer, for example, by a photoetching technique in order to expose the given surface of the source and drain electrode if the TFT's produced are intended for use as a display panel. Due to this photoetching step, the TFT's, suffering from the peeling or contamination of the semiconducting layer, cannot show stable and reliable performance.

The conventional methods for fabricating the TFT based on the photolithography method are not always aimed at the application of the TFT array to display devices and are those that are not directly applicable to this purpose.

The reason why the photolithography method most popularly adopted in silicon IC technology has not yet yielded a satisfactory solution in the fabrication of the TFT's seems to be due mainly to the fact that in addition to the difficulty in the precise photoetching of large size devices, the contamination during the etching process and the complexity of the processes, a practical production method has not yet been developed both in materials and processes.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a practical production method of a thin film transistor array of uniformly high density using relatively few processes.

This object is achieved according to this invention by the providing of a method which includes:

a step of forming a first electrode layer almost uniformly on a insulating substrate;

a step of patterning the first electrode layer into a source electrode, drain electrode, bus bar electrode, or one or both of the electrodes used for a passive element such as resistor or capacitor;

a step of uniformly depositing a semiconducting layer, under vacuum, on the surface of the substrate having the first electrode layer with a given shape;

a step of uniformly depositing an insulating layer on the whole surface of the semiconducting layer;

a step of patterning the insulating layer into desired shape by means of a photoetching process;

a step of subsequently photoetching the semiconducting layer into the same shape as that of the insulating layer;

a step of uniformly depositing a second electrode layer on the exposed surfaces of the insulating layer and the first electrode layer on the substrate; and

a step of patterning the second electrode layer into the shape of a gate electrode, bus connection electrode or electrodes used for a resistor or capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

This and other objects and features of this invention will be apparent from the descriptions herein and the accompanying drawings, in which:

FIG. **1** is a cross-sectional view of a portion of a thin film transistor array according to a conventional method;

FIG. **2** is a cross-sectional view of a portion of a thin film transistor array according to another conventional method;

FIG. **3** is a plan view, at the second step of the production process, of a portion of a thin film transistor array according to an example of a method of this invention;

FIG. **4** is a plan view of a portion of a thin film transistor array according to the example of the method of this invention, which portion corresponds to that indicated by the dotted circle in FIG. **3**;

FIG. **5** is a cross-sectional view of a portion of a thin film transistor array according to an elementary example of the method of this invention;

FIG. **6** is a cross-sectional view of a portion of a thin film transistor array according to an example of the method of this invention improved over the elementary example of FIG. **5**; and

FIG. **7** is a plan view of a portion of a thin film transistor array according to the improved example of the method of this invention as of FIG. **6**, which portion corresponds to that indicated by the dotted circle in FIG. **3**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

This invention will be described hereinafter with the aid of the accompanying drawings. As described above, a transparent electrode, such as indium oxide or tin oxide or indium tin oxide is at first deposited, to a thickness of 200 Å to 1000 Å, on an insulating substrate such as glass in order to form the first electrode layer.

In the second step, using a well known photoresist, such as phenolnovolak resin, the first electrode layer is patterned as shown in FIG. **3** into the shape of a source electrode **4**, drain electrode **5**, bus bar electrodes **7-1**, **7-2** or, if necessary, one or both of the electrodes used for a resistor or capacitor. (These latter electrodes are omitted in FIG. **3** for simplicity of explanation). A dilute hydrochloric acid can be used as the etching solution for the first electrode such as indium oxide, tin oxide or indium tin oxide.

After removing the photoresist remaining on the patterned **1**st electrodes **4**, **5**, **7-1**, **7-2** and carefully cleaning and drying the substrate, in the third step a semiconducting material such as cadmium selenide, cadmium sulfide, lead sulfide, or tellurium is uniformly deposited by vacuum evaporation or sputtering, to a thickness of 50 Å to 2000 Å, to form the semiconducting layer.

Successively after deposition of the semiconducting layer, in the fourth step, an insulating layer such as aluminum oxide, silicon nitride and silicon oxide is deposited uniformly by vacuum evaporation or sputtering techniques to a thickness of from 0.1 μm to 0.6 μm over the semiconducting layer. After taking out the substrate **3**, from the vacuum bell jar, with the semiconducting layer and the insulating layer deposited thereon, in the fifth step, the photoresist, after being uniformly coated over the insulating layer on the substrate **3**, is photoetched into the shapes corresponding to those of the gate insulating layer **1** and crossover insulating layer **8**. The substrate **3** with the given pattern of the photoresist layer thereon is then exposed to the etching solution or etching gas so that the unnecessary portions of the insu-

lating layer is removed by etching. When the insulating layer **1** or **8** is composed of aluminum oxide, a hot phosphoric acid (about 60° C.) is suitable for etching the aluminum oxide. The etching rate is about 30 Å/S at 60° C. In the sixth step, the substrate **3** is exposed to the etching solution or etching gas as well as in the fifth step except that in this step, the etching solution or gas appropriate for the semiconducting layer **2** or **9** is used. When cadmium selenide is used as the semiconducting layer, it has been found that 0.1–0.7wt% aqueous solution of bromine is effectively suitable as the etching solution for the cadmium selenide. The etching rate of the CdSe is about 15 Å/s at 20° C. with an etching solution of 0.35wt%.

During the steps described above, a substrate **3** is obtained which has a double layer of the semiconducting layer **2**(or **9**) and insulating layer **1**(or **8**) thereon with the same shape covering given portions of the source electrode **4** and drain electrode **5** and covering given portions of the bus bar electrode **7-2** for use as crossover insulation. Here, the semiconducting layer **9** under the insulating layer **8** at the portion of the crossover insulation does not function as a semiconductor element.

After removing the photoresist remaining on the surfaces of the insulating layer **1**, **8** and carefully cleaning the substrate **3**, in the seventh step, the second electrode material is deposited uniformly on almost the whole surface of the side of the substrate **3** having the layers of the first electrodes **4**, **5**, **7-1**, **7-2**, semiconductors **2**, **9** (these are not exposed and covered by the insulating layers **1**, **8**) and insulating layers **2**, **9**.

Metallic aluminum or chromium is suitable as the material for the second electrode. Electrode materials such as gold, indium oxide and tin oxide are not appropriate for the second electrode because the etching solutions or gas used for those electrode materials are apt to deteriorate the semiconductor and the insulators **1**, **8** for the gate or the crossover insulation, respectively.

In the eighth step, the second electrode layer is photoetched into a given pattern so as to form the gate electrode **6**, connection electrodes **7-3** for the electrical connections of the bus bar electrode **7-1**, and either a resistor or capacitor (not shown in the drawings). Here, the electrode **7-4**, deposited on the electrode **7-1** or **7-2**, serves both to mechanically and electrically strengthen those electrodes **7-1** and **7-2**.

The photoresist layer remaining on the surface of the gate electrode **6**, and connection electrodes **7-4** and **7-3** does not have to be removed but after being hardened by appropriate heat treatment, serves to protect the surfaces of these electrodes.

In the steps described above, the formation of crossover insulation layer **8** is completed simultaneously with the formation of the gate insulator **1** and semiconductor **2** for the TFT's. However, when the high voltage operation of the TFT array is required, the basic process described above can be modified. It is more desirable to form an electrically more stable and reliable insulating layer with sufficient thickness for use as a crossover insulation layer and capacitance layer. In this case, an additional process is required to form a thick insulating layer for crossover insulator or capacitor, either before the third step or before the second step described above.

As an insulator material for this purpose, a metal oxide such as aluminum oxide or cerium oxide or an organic polymer such as a photoresist can be utilized. According to our experiments, a metal oxide layer with a thickness of about 1 μm or a photoresist layer with a thickness of about 2 μm is satisfactory for use as the electrical insulation for a voltage strength more than 50 volts. Both insulator materials can be easily patterned into a desired shape by at first forming a uniform layer by vacuum evaporation, sputtering, spraying and so on and then photoetching it into a given pattern.

In the performance of the TFT's, since a thick gate insulator requires a high gate voltage for obtaining the desired drain current, the thin gate insulator is the preferable. However, for the applications using a high gate voltage, a gate insulator thicker than 0.6 μm is desirable.

It has also been found that the TFT's obtained by the present method based on a photoetching process can be improved by other modifications. The cross section of the TFT fabricated by the basic method is shown in FIG. **5**. There is an undulation in the semiconductor, gate insulator and gate electrode at the edges of the source and drain electrode **4** and **5** due to the thickness of those electrodes. The existence of this undulation, which is apt to give some damage to the semiconducting layer **2** or insulating layer **1** during the steps of etching the photoresist, insulator and semiconductor layers, might cause undesired side etching, cracking or peeling of the semiconducting layer and/or insulating layer during such etching steps. Then, according to this invention, this undulation is removed by depositing an insulating layer **10** with almost same thickness as that of the first electrode between the electrodes of the source and the drain and at the crossing portion of the bus bar electrode as shown in FIGS. **6** and **7**. Thereby, a good effect can be obtained in the production yield of the TFT array and the precision of the shape of the semiconductor **2**, **9** and insulator **1**, **8**. Furthermore, the additional advantage has been obtained by providing the insulating layer **10** for removing the undulation. The advantage is that the TFT produced with this insulating layer **10** shows a higher off-resistance and higher on/off ratio of the drain current than that produced without it. Though the reason is not clear at present, this effect is considered to be caused perhaps by the reduction of the amount of the induced charge in the semiconductor resulting from the contact with the deposited insulating layer **10**.

As described above, though the provision of another insulating layer for the diminishment of undulation results in an increase in production steps, the step used to deposit the insulating layer on the whole substrate having the source and drain electrodes with a given shape and the step used to photoetch the insulating layer into a given pattern, enables the obtaining of a high production yield and better performance of the TFT array.

As the insulating layer **10**, aluminum oxide has been found to be preferable.

As apparent from the foregoing, according to the basic method according to this invention for producing a TFT array in which a crossover insulator is formed at the same time as the formation of the semiconducting layer **2** and the insulating layer **1**, putting-in and taking-out of the substrate **3** to and from the vacuum vessel are carried out three times; coating, exposing and developing of photoresist layers are carried out three times; photoetching of the electrodes is carried out twice; photoetching of the insulator and semiconducting layer is carried out once, respectively. Though it is not appropriate to say that the present method comprises very few steps, this method does not require any special care

except for the setting of the photomask for the exposure of the photoresist to the light pattern and never requires the delicate setting of a metal mask to the substrate for vacuum evaporation with a given pattern. Therefore, the present method ultimately can result in a high production rate by the simultaneous treatment of many substrates, and has a capability of fabricating, without difficulty, a TFT array with the density of more than 100 lines/inch.

The smallest size TFT having been fabricated so far on the basis of the present invention has a channel length dimension of 10 μm and a channel width of 20 μm, and has shown excellent TFT characteristics such as an on/off ratio of drain current which is more than 10^4. The TFT's produced by the present method generally show high on/off drain currents. For an application requiring extremely low off current (<10 nA), the post heat treatment (at 200° C. for about 2 hours) of the array is preferable for reducing the off-current and obtaining a higher on/off ratio of the drain current. According to the present method, it has also been found that it is possible to relatively easily fabricate a TFT array having a precision of the order of tens of μm with respect to the electrodes for the gate, source, drain and bus bar, gate and crossover insulators, and channel semiconductor uniformly on a substrate which is more than 10 cm×10 cm in size.

Further advantages in the present method are as follows.

Especially in a field effect transistor, the boundary between the gate insulating layer **1** and the semiconducting layer **2** has a remarkable effect upon the characteristics of the TFT produced. If there are mobile ions, polarizable impurities and/or a trapping state of charges are present at the boundary, the stable and excellent performance of the TFT may not be expected. Therefore, it is preferable to keep the boundary between the semiconducting layer **2** and the insulating layer **1** very clean and free from contamination. According to the present method, since the semiconducting layer **2** and insulating layer **1** are successively deposited under high vacuum, this delicate boundary layer can be prevented from contamination.

It has also been found that the electrode material such as the indium oxide or tin oxide, or indium tin oxide makes an ohmic contact to the cadmium selenide semiconducting layer. Therefore, it is possible to use such transparent conducting materials directly as the source and drain electrodes **4** and **5**. This brings about an advantage in that a transmissive-type display device utilizing liquid crystal techniques can be easily fabricated by fewer steps. If an opaque metal electrode must be utilized as the source and drain electrode for achieving the ohmic contact with the semiconducting layer, an additional process for providing a transparent electrode electrically connected to the source or drain electrode becomes necessary for the fabrication of a TFT array used for a transmissive type display device.

According to the present invention which does not need the use of a metal mask during vacuum evaporation, the substrate can be heated during evaporation because concern for the difference in the thermal expansion between the substrate and metal mask is unnecessary. The heating of the substrate during the evaporation generally results in a better performance of the fabricated TFT's mainly by the excellent adhesion of the evaporated material to the substrate, an improvement in the electrical durability of the insulating material for gate insulator or crossover insulation layer, and a capability of the control of the electrical resistance of the semiconducting layer.

In the foregoing description, the present invention's method of producing the TFT array has been explained mainly for the purpose of producing the switching array for the display panel. However, the present invention is not limited to that application but is applicable to any other thin film active circuits consisting of TFT active elements, thin film resistor and thin film capacitors such as the driving circuits for a display panel.

What is claimed is:

1. A method producing a thin film transistor comprising: uniformly forming a first electrode layer over an insulating substrate; forming electrodes for at least one of source, drain, and interconnecting lines with desired patterns by photoetching said first electrode layer; forming a uniform semiconducting layer on a surface of the substrate having said patterned electrodes; successively forming a uniform insulating layer over said uniform semiconducting layer; photoetching said uniform insulating layer into a desired pattern; photoetching said uniform semiconducting layer into the same pattern as said patterned insulating layer; forming a second electrode uniformly over the surface having said patterned electrode and insulating layer; and photoetching said uniformly deposited second electrode into a desired pattern.

2. A method of producing a thin film transistor as claimed in claim **1**, wherein said first electrode is made of a conductive electrode material selected from the group consisting of indium oxide, tin oxide and indium tin oxide.

3. A method of producing a thin film transistor as claimed in claim **1**, comprising a further step, effected between said electrode forming step and said semiconducting layer forming step, of forming an insulating layer with a given shape and substantially the same thickness as said first electrode, at least on the portion of the substrate where said first electrode layer has been partially removed, and wherein the semiconducting layer and insulating layer having given shapes are to be provided in successive steps.

4. A method of producing a thin film transistor as claimed in claim **1**, comprising a further step, effected between said electrode forming step and said semiconducting layer forming step, of forming an insulating layer by means of either a vacuum evaporation or sputtering method.

5. A method of producing a thin film transistor as claimed in claim **1**, comprising a further step, effected between said semiconducting layer photoetching step and said second electrode forming step, of forming an insulating layer by means of either a vacuum evaporation or sputtering method.

6. A method of producing thin film transistor as claimed in claim **4** or **5**, wherein said insulating layer is made of a photosensitive organic polymer.

7. A method of producing a thin film transistor as claimed in claim **1**, wherein said semiconducting layer material is made of cadmium selenide.

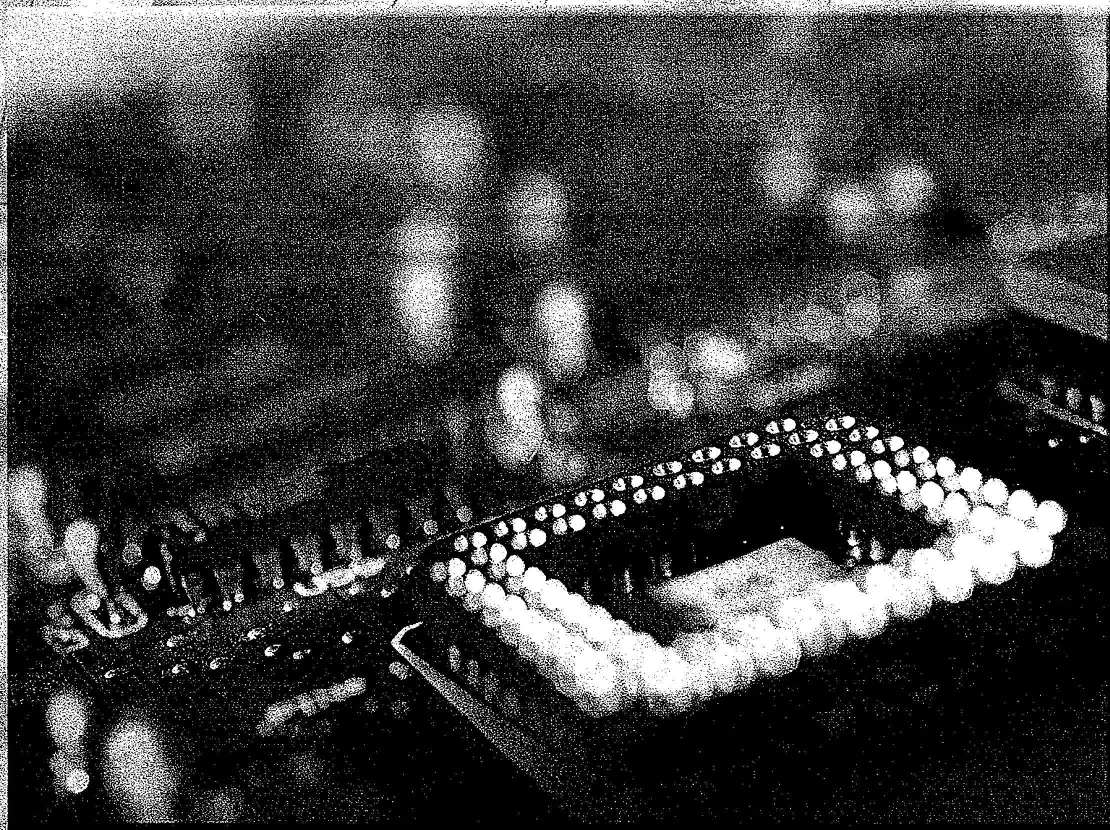
8. A method of producing a thin film transistor as claimed in claim **7**, wherein an etching solution used for photoetching said semiconducting layer material is an aqueous solution of from 0.1 to 0.7wt.% of bromine.

9. A method of producing a thin film transistor as claimed in claim **1**, **3**, **4** or **5**, wherein said insulating layer is made of aluminum oxide.

10. A method of producing a thin film transistor as claimed in claim **9**, wherein an etching solution used for photoetching said insulating layer is hot phosphoric acid.

* * * * *

EXHIBIT A-4



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Basic Principles

Donald A. Neamen

Third Edition

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CHAPTER 11

Fundamentals of the Metal–Oxide–Semiconductor Field-Effect Transistor

PREVIEW

The fundamental physics of the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) is developed in this chapter. Although the bipolar transistor was discussed in the last chapter, the material in this chapter presumes a knowledge only of the semiconductor material properties and characteristics of the pn junction.

The MOSFET, in conjunction with other circuit elements, is capable of voltage gain and signal-power gain. The MOSFET is also used extensively in digital circuit applications where, because of its relatively small size, thousands of devices can be fabricated in a single integrated circuit. The MOSFET is, without doubt, the core of integrated circuit design at the present time.

The MOS designation is implicity used only for the metal–silicon dioxide (SiO_2)–silicon system. The more general terminology is metal–insulator–semiconductor (MIS), where the insulator is not necessarily silicon dioxide and the semiconductor is not necessarily silicon. We will use the MOS system throughout this chapter although the same basic physics applies to the MIS system.

The heart of the MOSFET is a metal–oxide–semiconductor structure known as an MOS capacitor. The energy bands in the semiconductor near the oxide–semiconductor interface bend as a voltage is applied across the MOS capacitor. The position of the conduction and valence bands relative to the Fermi level at the oxide–semiconductor interface is a function of the MOS capacitor voltage, so that the characteristics of the semiconductor surface can be inverted from p-type to n-type, or from n-type to p-type, by applying the proper voltage. The operation and characteristics of the MOSFET are dependent on this inversion and the creation of

an inversion charge density at the semiconductor surface. The threshold voltage is defined as the applied gate voltage required to create the inversion layer charge and is one of the important parameters of the MOSFET.

The various types of MOSFETs are examined and a qualitative discussion of the current–voltage characteristics is initially presented. A mathematical derivation of the current–voltage relation is then covered in detail. The frequency response and limitations of the MOSFET are also considered.

Although we have not discussed fabrication processes in any detail in this text, there is an MOS technology that should be considered, since it directly influences the characteristics and properties of the MOS devices and circuits. We will consider the complementary MOS (CMOS) process. The discussion of this technology will be brief, but should provide a good base for further in-depth study. ■

11.1 | THE TWO-TERMINAL MOS STRUCTURE

The heart of the MOSFET is the metal–oxide–semiconductor capacitor shown in Figure 11.1. The metal may be aluminum or some other type of metal, although in many cases, it is actually a high-conductivity polycrystalline silicon that has been deposited on the oxide; however, the term metal is usually still used. The parameter t_{ox} in the figure is the thickness of the oxide and ϵ_{ox} is the permittivity of the oxide.

11.1.1 Energy-Band Diagrams

The physics of the MOS structure can be more easily explained with the aid of the simple parallel-plate capacitor. Figure 11.2a shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates as shown. The capacitance per unit area for this geometry is

$$C' = \frac{\epsilon}{d} \tag{11.1}$$

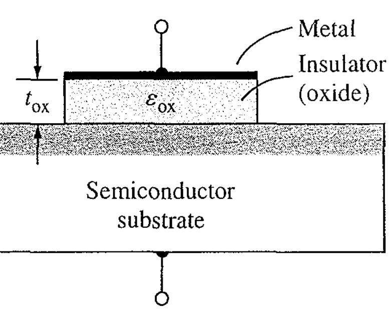


Figure 11.1 | The basic MOS capacitor structure.

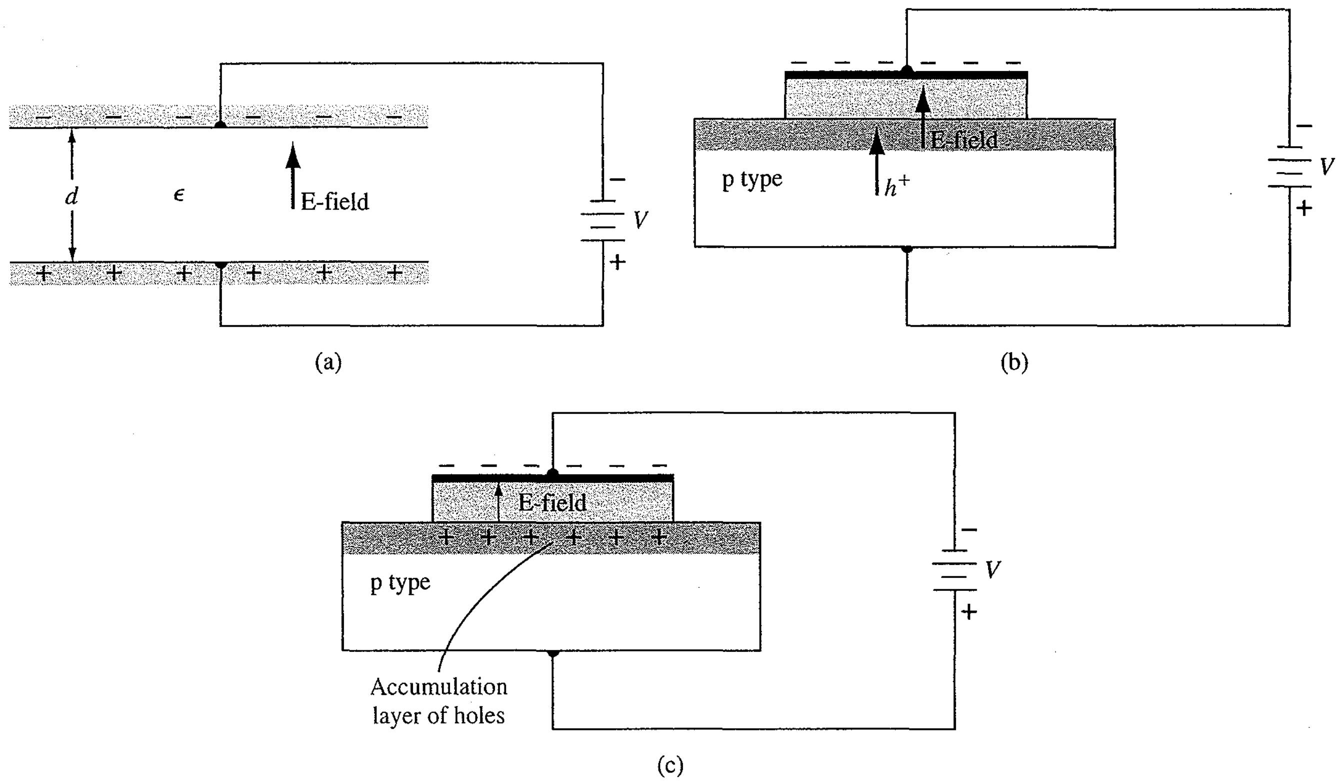


Figure 11.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

where ϵ is the permittivity of the insulator and d is the distance between the two plates. The magnitude of the charge per unit area on either plate is

$$Q' = C'V \tag{11.2}$$

where the prime indicates charge or capacitance per unit area. The magnitude of the electric field is

$$\mathrm{E} = \frac{V}{d} \tag{11.3}$$

Figure 11.2b shows an MOS capacitor with a p-type semiconductor substrate. The top metal gate is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure. If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide–semiconductor interface. Figure 11.2c shows the equilibrium distribution of charge in the MOS capacitor with this particular applied voltage. An *accumulation layer* of holes in the oxide–semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

E11.10 Consider an MOS device with the following parameters: p^+ polysilicon gate, n-type substrate with $N_d = 10^{15}$ cm^{-3}, $t_{ox} = 220$ Å, and $Q'_{ss} = 8 \times 10^{10}$ cm^{-2}. (Use Figure 11.15). Determine the threshold voltage. (Ans. $V_{TP} = +0.224$ V)

***E11.11** The device described in E11.10 is to be redesigned by changing the n-type doping concentration such that the threshold voltage is in the range $-0.50 \le V_{TP} \le -0.30$ V. (Ans. By trial and error, $V_{TP} = -0.405$ V for $N_d = 4 \times 10^{16}$ cm^{-3})

11.2 | CAPACITANCE–VOLTAGE CHARACTERISTICS

The MOS capacitor structure is the heart of the MOSFET. A great deal of information about the MOS device and the oxide–semiconductor interface can be obtained from the capacitance versus voltage or *C-V* characteristics of the device. The capacitance of a device is defined as

$$C = \frac{dQ}{dV} \tag{11.30}$$

where dQ is the magnitude of the differential change in charge on one plate as a function of the differential change in voltage dV across the capacitor. The capacitance is a small-signal or ac parameter and is measured by superimposing a small ac voltage on an applied dc gate voltage. The capacitance, then, is measured as a function of the applied dc gate voltage.

11.2.1 Ideal *C-V* Characteristics

First we will consider the ideal *C-V* characteristics of the MOS capacitor and then discuss some of the deviations that occur from these idealized results. We will initially assume that there is zero charge trapped in the oxide and also that there is no charge trapped at the oxide–semiconductor interface.

There are three operating conditions of interest in the MOS capacitor: accumulation, depletion, and inversion. Figure 11.24a shows the energy-band diagram of an MOS capacitor with a p-type substrate for the case when a negative voltage is applied to the gate, inducing an accumulation layer of holes in the semiconductor at the oxide-semiconductor interface. A small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in the hole accumulation charge, as shown in Figure 11.24b. The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor. The capacitance C' per unit area of the MOS capacitor for this accumulation mode is just the oxide capacitance, or

$$C'(\text{acc}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{11.31}$$

Figure 11.25a shows the energy-band diagram of the MOS device when a small positive voltage is applied to the gate, inducing a space charge region in the semiconductor; Figure 11.25b shows the charge distribution through the device for

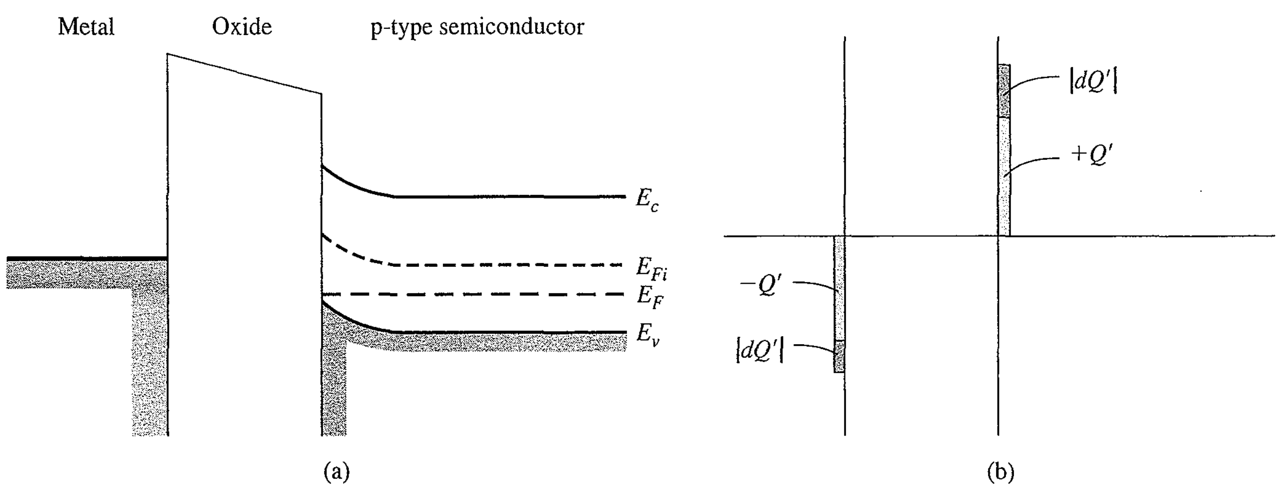


Figure 11.24 | (a) Energy-band diagram through an MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

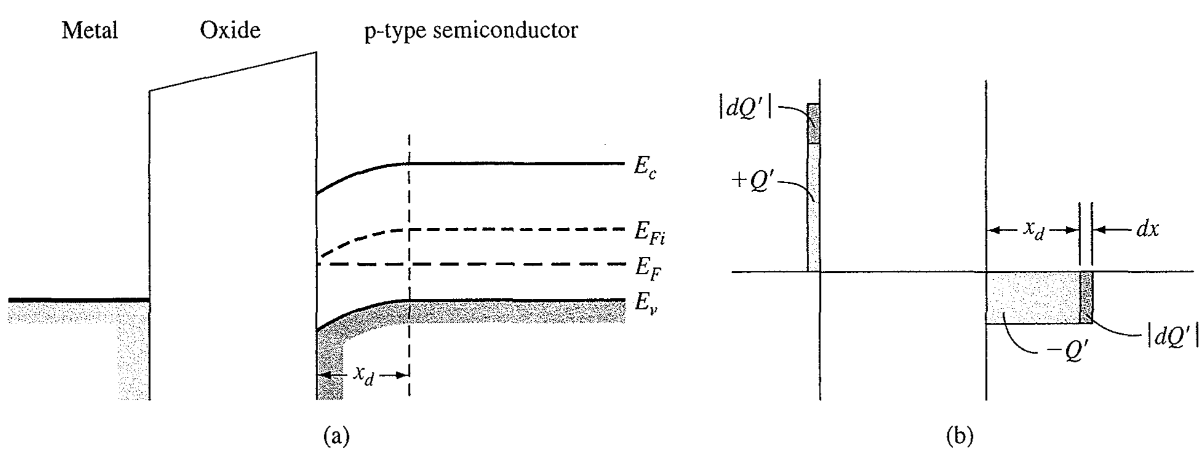


Figure 11.25 | (a) Energy-band diagram through an MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

this condition. The oxide capacitance and the capacitance of the depletion region are in series. A small differential change in voltage across the capacitor will cause a differential change in the space charge width. The corresponding differential changes in charge densities are shown in the figure. The total capacitance of the series combination is

$$\frac{1}{C'(\text{depl})} = \frac{1}{C_{\text{ox}}} + \frac{1}{C'_{SD}} \tag{11.32a}$$

or

$$C'(\text{depl}) = \frac{C_{\text{ox}} C'_{SD}}{C_{\text{ox}} + C'_{SD}} \tag{11.32b}$$

Since $C_{ox} = \epsilon_{ox}/t_{ox}$ and $C'_{SD} = \epsilon_s/x_d$, Equation (11.32b) can be written as

$$C'(\text{depl}) = \frac{C_{ox}}{1 + \dfrac{C_{ox}}{C'_{SD}}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right) x_d} \tag{11.33}$$

As the space charge width increases, the total capacitance $C'(\text{depl})$ decreases.

We had defined the threshold inversion point to be the condition when the maximum depletion width is reached but there is essentially zero inversion charge density. This condition will yield a minimum capacitance $C'_{\min}$ which is given by

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}} \tag{11.34}$$

Figure 11.26a shows the energy-band diagram of this MOS device for the inversion condition. In the ideal case, a small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density. The space charge width does not change. If the inversion charge can respond to the change in capacitor voltage as indicated in Figure 11.26b, then the capacitance is again just the oxide capacitance, or

$$C'(\text{inv}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{11.35}$$

Figure 11.27 shows the ideal capacitance versus gate voltage, or C-V, characteristics of the MOS capacitor with a p-type substrate. The three dashed segments correspond to the three components C_{ox}, C'_{SD}, and $C'_{\min}$. The solid curve is the ideal net capacitance of the MOS capacitor. Moderate inversion, which is indicated in the figure, is the transition region between the point when only the space charge density

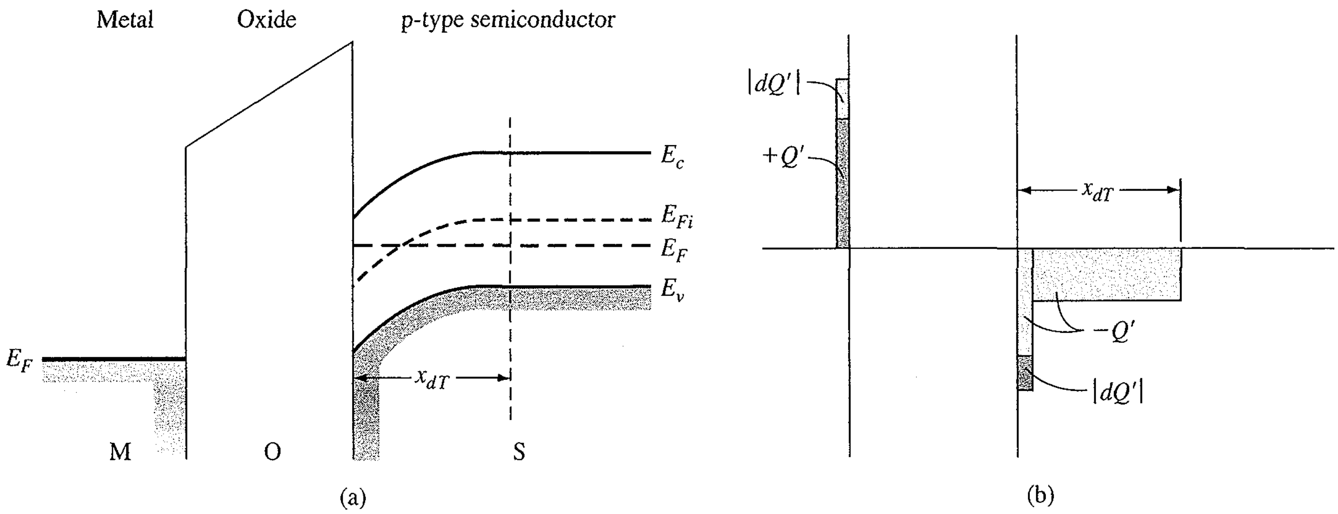


Figure 11.26 | (a) Energy-band diagram through an MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

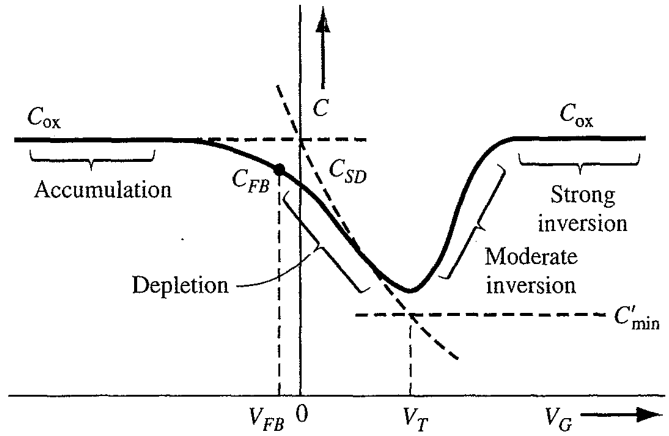


Figure 11.27 | Ideal low-frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

changes with gate voltage and when only the inversion charge density changes with gate voltage.

The point on the curve that corresponds to the flat-band condition is of interest. The flat-band condition occurs between the accumulation and depletion conditions. The capacitance at flat band is given by

$$\boxed{C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\dfrac{kT}{e}\right)\left(\dfrac{\epsilon_s}{eN_a}\right)}}} \tag{11.36}$$

We may note that the flat-band capacitance is a function of oxide thickness as well as semiconductor doping. The general location of this point on the *C-V* plot is shown in Figure 11.27.

EXAMPLE 11.7

Objective

To calculate C_{ox}, C'_{min}, and C'_{FB} for an MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The oxide is silicon dioxide with a thickness of 550 Å and the gate is aluminum.

■ Solution

The oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{550 \times 10^{-8}} = 6.28 \times 10^{-8} \text{ F/cm}^2$$

To find the minimum capacitance, we need to calculate

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.347 \text{ V}$$

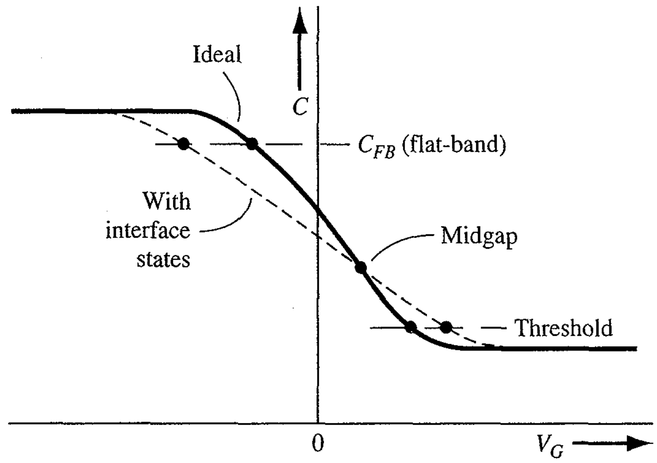


Figure 11.34 | High-frequency *C-V* characteristics of an MOS capacitor showing effects of interface states.

particular bias condition is known as *midgap*. Figure 11.33c shows the condition at inversion in which there is now a net negative charge in the acceptor states.

The net charge in the interface states changes from positive to negative as the gate voltage sweeps from the accumulation, depletion, to the inversion condition. We noted that the *C-V* curves shifted in the negative gate voltage direction due to positive fixed oxide charge. When interface states are present, the amount and direction of the shift changes as we sweep through the gate voltage, since the amount and sign of the interface trapped charge changes. The *C-V* curves now become "smeared out" as shown in Figure 11.34.

Again, the *C-V* measurements can be used as a diagnostic tool in semiconductor device process control. For a given MOS device, the ideal *C-V* curve can be determined. Any "smearing out" in the experimental curve indicates the presence of interface states and any parallel shift indicates the presence of fixed oxide charge. The amount of smearing out can be used to determine the density of interface states. These types of measurement are extremely useful in the study of radiation effects on MOS devices, which we will consider in the next chapter.

11.3 | THE BASIC MOSFET OPERATION

The current in an MOS field-effect transistor is due to the flow of charge in the inversion layer or channel region adjacent to the oxide-semiconductor interface. We have discussed the creation of the inversion layer charge in enhancement-type MOS capacitors. We may also have depletion-type devices in which a channel already exists at zero gate voltage.

11.3.1 MOSFET Structures

There are four basic MOSFET device types. Figure 11.35 shows an n-channel enhancement mode MOSFET. Implicit in the enhancement mode notation is the idea

that the semiconductor substrate is not inverted directly under the oxide with zero gate voltage. A positive gate voltage induces the electron inversion layer, which then "connects" the n-type source and the n-type drain regions. The source terminal is the source of carriers that flow through the channel to the drain terminal. For this n-channel device, electrons flow from the source to the drain so the conventional current will enter the drain and leave the source. The conventional circuit symbol for this n-channel enhancement mode device is also shown in this figure.

Figure 11.36 shows an n-channel depletion mode MOSFET. An n-channel region exists under the oxide with zero volts applied to the gate. However, we have shown that the threshold voltage of an MOS device with a p-type substrate may be

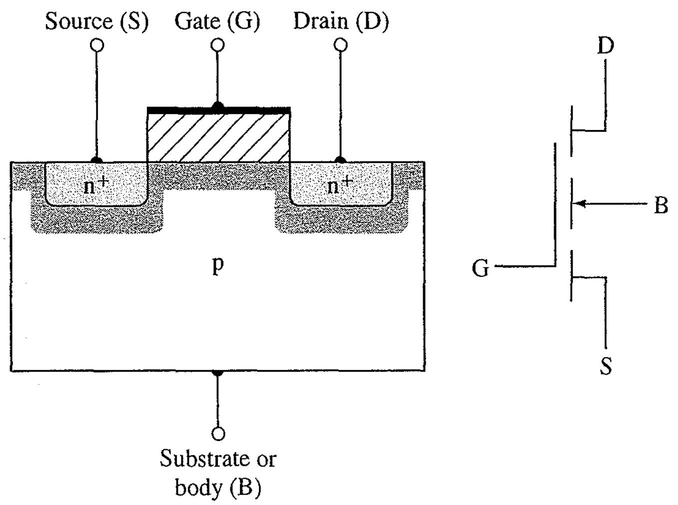


Figure 11.35 | Cross section and circuit symbol for an n-channel enhancement-mode MOSFET.

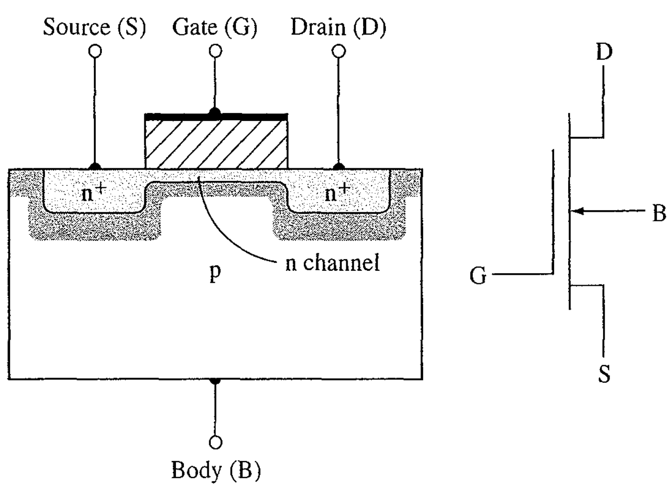
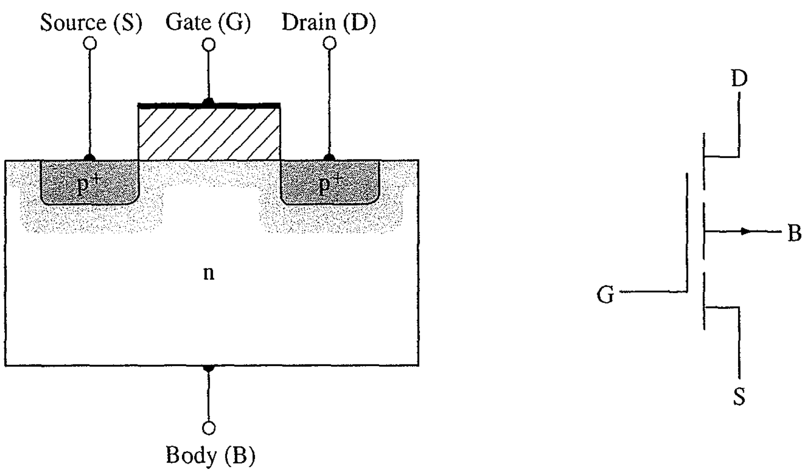


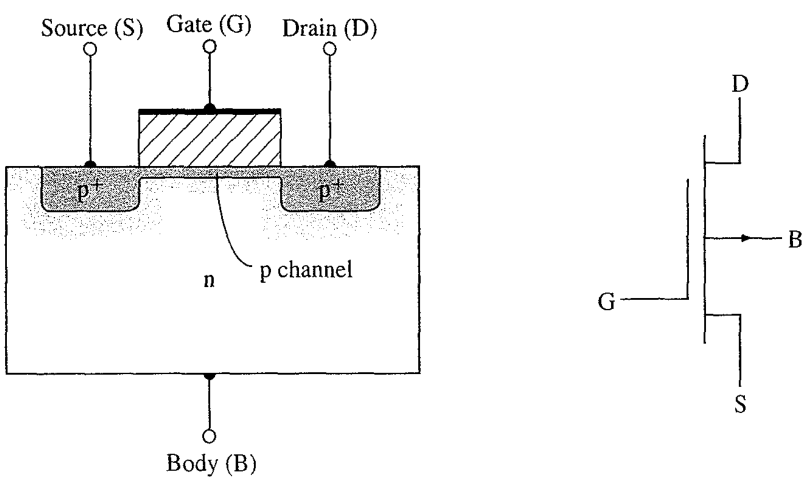
Figure 11.36 | Cross section and circuit symbol for an n-channel depletion-mode MOSFET.

negative; this means that an electron inversion layer already exists with zero gate voltage applied. Such a device is also considered to be a depletion mode device. The n-channel shown in this figure can be an electron inversion layer or an intentionally doped n-region. The conventional circuit symbol for the n-channel depletion mode MOSFET is also shown in the figure.

Figures 11.37a and 11.37b show a p-channel enhancement mode MOSFET and a p-channel depletion mode MOSFET. In the p-channel enhancement mode device, a negative gate voltage must be applied to create an inversion layer of holes that will "connect" the p-type source and drain regions. Holes flow from the source to the drain, so the conventional current will enter the source and leave the drain. A p-channel region exists in the depletion mode device even with zero gate voltage. The conventional circuit symbols are shown in the figure.



(a)



(b)

Figure 11.37 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET and (b) a p-channel depletion mode MOSFET.

APPENDIX A

Selected List of Symbols

This list does not include some symbols that are defined and used specifically in only one section. Some symbols have more than one meaning; however, the context in which the symbol is used should make the meaning unambiguous. The usual unit associated with each symbol is given.

a	Unit cell dimension (Å), potential well width, acceleration, gradient of impurity concentration, channel thickness of a one-sided JFET (cm)
a_0	Bohr radius (Å)
c	Speed of light (cm/s)
d	Distance (cm)
e	Electronic charge (magnitude) (C), Napierian base
f	Frequency (Hz)
$f_F(E)$	Fermi–Dirac probability function
f_T	Cutoff frequency (Hz)
g	Generation rate ($\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$)
g'	Generation rate of excess carriers ($\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$)
$g(E)$	Density of states function ($\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$)
g_c, g_v	Density of states function in the conduction band and valence band ($\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$)
g_d	Channel conductance (S), small-signal diffusion conductance (S)
g_m	Transconductance (A/V)
g_n, g_p	Generation rate for electrons and holes ($\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$)
h	Planck's constant (J-s), induced space charge width in a JFET (cm)
$\hbar$	Modified Planck's constant ($h/2\pi$)

h_f	Small-signal common emitter current gain
j	Imaginary constant, $\sqrt{-1}$
k	Boltzmann's constant (J/K), wavenumber (cm^{-1})
k_n	Conduction parameter (A/V^2)
m	Mass (kg)
m_0	Rest mass of the electron (kg)
m^*	Effective mass (kg)
m_n^*, m_p^*	Effective mass of an electron and hole (kg)
n	Integer
n, l, m, s	Quantum numbers
n, p	Electron and hole concentration (cm^{-3})
$\bar{n}$	Index of refraction
n', p'	Constants related to the trap energy (cm^{-3})
n_{B0}, p_{E0}, p_{C0}	Thermal-equilibrium minority carrier electron concentration in the base and minority carrier hole concentration in the emitter and collector (cm^{-3})
n_d	Density of electrons in the donor energy level (cm^{-3})
n_i	Intrinsic concentration of electrons (cm^{-3})
n_0, p_0	Thermal-equilibrium concentration of electrons and holes (cm^{-3})
n_p, p_n	Minority carrier electron and minority carrier hole concentration (cm^{-3})
n_{p0}, p_{n0}	Thermal-equilibrium minority carrier electron and minority carrier hole concentration (cm^{-3})
n_s	Density of a two-dimensional electron gas (cm^{-2})
p	Momentum
p_a	Density of holes in the acceptor energy level (cm^{-3})
p_i	Intrinsic hole concentration ($= n_i$)(cm^{-3})
q	Charge (C)
r, θ, ϕ	Spherical coordinates
r_d, r_π	Small-signal diffusion resistance (Ω)
r_{ds}	Small-signal drain-to-source resistance (Ω)
s	Surface recombination velocity (cm/s)
t	Time (s)
t_d	Delay time (s)
t_{ox}	Gate oxide thickness (cm or Å)
t_s	Storage time (s)
$u(x)$	Periodic wave function
v	Velocity (cm/s)
v_d	Carrier drift velocity (cm/s)

$v_{ds}, v_s, v_{\text{sat}}$	Carrier saturation drift velocity (cm/s)
x, y, z	Cartesian coordinates
x	Mole fraction in compound semiconductors
x_B, x_E, x_C	Neutral base, emitter, and collector region widths (cm)
x_d	Induced space charge width (cm)
x_{dT}	Maximum space charge width (cm)
x_n, x_p	Depletion width from the metallurgical junction into n-type and p-type semiconductor regions (cm)
A	Area (cm^2)
A^*	Effective Richardson constant ($\text{A/K}^2/\text{cm}^2$)
B	Magnetic flux density (Wb/m^2)
B, E, C	Base, emitter, and collector
BV_{CBO}	Breakdown voltage of collector-base junction with emitter open (volt)
BV_{CEO}	Breakdown voltage of collector-emitter with base open (volt)
C	Capacitance (F)
C'	Capacitance per unit area (F/cm^2)
C_d, C_π	Diffusion capacitance (F)
C_{FB}	Flat-band capacitance (F)
C_{gs}, C_{gd}, C_{ds}	Gate-source, gate-drain, and drain-source capacitance (F)
C'_j	Junction capacitance per unit area (F/cm^2)
C_M	Miller capacitance (F)
C_n, C_p	Constants related to capture rate of electrons and holes
C_{ox}	Gate oxide capacitance per unit area (F/cm^2)
C_μ	Reverse-biased B-C junction capacitance (F)
D, S, G	Drain, source, and gate of an FET
D'	Ambipolar diffusion coefficient (cm^2/s)
D_B, D_E, D_C	Base, emitter, and collector minority carrier diffusion coefficients (cm^2/s)
D_{it}	Density of interface states ($\#/\text{eV-cm}^3$)
D_n, D_p	Minority carrier electron and minority carrier hole diffusion coefficient (cm^2/s)
E	Energy (joule or eV)
E_a	Acceptor energy level (eV)
E_c, E_v	Energy at the bottom edge of the conduction band and top edge of the valence band (eV)
$\Delta E_c, \Delta E_v$	Difference in conduction band energies and valence band energies at a heterojunction (eV)
E_d	Donor energy level (eV)

E_F	Fermi energy (eV)
E_{Fi}	Intrinsic Fermi energy (eV)
E_{Fn}, E_{Fp}	Quasi-Fermi energy levels for electrons and holes (eV)
E_g	Bandgap energy (eV)
ΔE_g	Bandgap narrowing factor (eV), difference in bandgap energies at a heterojunction (eV)
E_t	Trap energy level (eV)
F	Force (N)
F_n^-, F_p^+	Electron and hole particle flux (cm^{-2} s^{-1})
$F_{1/2}(\eta)$	Fermi–Dirac integral function
G	Generation rate of electron-hole pairs (cm^{-3} s^{-1})
G_L	Excess carrier generation rate (cm^{-3} s^{-1})
G_{n0}, G_{p0}	Thermal equilibrium generation rate for electrons and holes (cm^{-3} s^{-1})
G_{01}	Conductance (S)
I	Current (A)
I_A	Anode current (A)
I_B, I_E, I_C	Base, emitter, and collector current (A)
I_{CBO}	Reverse-bias collector-base junction current with emitter open (A)
I_{CEO}	Reverse-bias collector–emitter current with base open (A)
I_D	Diode current (A), drain current (A)
I_D(sat)	Saturation drain current (A)
I_L	Photocurrent (A)
I_{P1}	Pinchoff current (A)
I_S	Ideal reverse-bias saturation current (A)
I_{SC}	Short-circuit current (A)
I_ν	Photon intensity (energy/cm^2/s)
J	Electric current density (A/cm^2)
J_{gen}	Generation current density (A/cm^2)
J_L	Photocurrent density (A/cm^2)
J_n, J_p	Electron and hole electric current density (A/cm^2)
J_n^-, J_p^+	Electron and hole particle current density (cm^{-2} s^{-1})
J_{rec}	Recombination current density (A/cm^2)
J_{r0}	Zero-bias recombination current density (A/cm^2)
J_R	Reverse-bias current density (A/cm^2)
J_S	Ideal reverse-bias saturation current density (A/cm^2)
J_{sT}	Ideal reverse saturation current density in a Schottky diode (A/cm^2)
L	Length (cm), inductance (H), channel length (cm)

ΔL	Channel length modulation factor (cm)
L_B, L_E, L_C	Minority carrier diffusion length in the base, emitter, and collector (cm)
L_D	Debye length (cm)
L_n, L_p	Minority carrier electron and hole diffusion length (cm)
M, M_n	Multiplication constant
N	Number density (cm^{-3})
N_a	Density of acceptor impurity atoms (cm^{-3})
N_B, N_E, N_C	Base, emitter, and collector doping concentrations (cm^{-3})
N_c, N_v	Effective density of states function in the conduction band and valence band (cm^{-3})
N_d	Density of donor impurity atoms (cm^{-3})
N_{it}	Interface state density (cm^{-2})
N_t	Trap density (cm^{-3})
P	Power (watt)
$P(r)$	Probability density function
Q	Charge (C)
Q'	Charge per unit area (C/cm^2)
Q_B	Gate controlled bulk charge (C)
Q'_n	Inversion channel charge density per unit area (C/cm^2)
Q'_{sig}	Signal charge density per unit area (C/cm^2)
$Q'_{SD}(\max)$	Maximum space charge density per unit area (C/cm^2)
Q'_{SS}	Equivalent trapped oxide charge per unit area (C/cm^2)
R	Reflection coefficient, recombination rate ($cm^{-3}\,s^{-1}$), resistance (Ω)
$R(r)$	Radial wave function
R_c	Specific contact resistance (Ω-cm^2)
R_{cn}, R_{cp}	Capture rate for electrons and holes ($cm^{-3}\,s^{-1}$)
R_{en}, R_{ep}	Emission rate for electrons and holes ($cm^{-3}\,s^{-1}$)
R_n, R_p	Recombination rate for electrons and holes ($cm^{-3}\,s^{-1}$)
R_{n0}, R_{p0}	Thermal equilibrium recombination rate of electrons and holes ($cm^{-3}\,s^{-1}$)
T	Temperature (K), kinetic energy (J or eV), transmission coefficient
V	Potential (volt), potential energy (J or eV)
V_a	Applied forward-bias voltage (volt)
V_A	Early voltage (volt), anode voltage (volt)
V_{bi}	Built-in potential barrier (volt)
V_B	Breakdown voltage (volt)
V_{BD}	Breakdown voltage at the drain (volt)

V_{BE}, V_{CB}, V_{CE}	Base-emitter, collector-base, and collector-emitter voltage (volt)
V_{DS}, V_{GS}	Drain-source and gate-source voltage (volt)
$V_{DS}(\text{sat})$	Drain-source saturation voltage (volt)
V_{FB}	Flat-band voltage (volt)
V_G	Gate voltage (volt)
V_H	Hall voltage (volt)
V_{oc}	Open-circuit voltage (volt)
V_{ox}	Potential difference across an oxide (volt)
V_{p0}	Pinchoff voltage (volt)
V_{pt}	Punch-through voltage (volt)
V_R	Applied reverse-bias voltage (volt)
V_{SB}	Source-body voltage (volt)
V_t	Thermal voltage (kT/e)
V_T	Threshold voltage (volt)
ΔV_T	Threshold voltage shift (volt)
W	Total space charge width (cm), channel width (cm)
W_B	Metallurgical base width (cm)
Y	Admittance
α	Photon absorption coefficient (cm^{-1}), ac common base current gain
α_n, α_p	Electron and hole ionization rates (cm^{-1})
α_0	dc common base current gain
α_T	Base transport factor
β	Common-emitter current gain
γ	Emitter injection efficiency factor
δ	Recombination factor
$\delta n, \delta p$	Excess electron and hole concentration (cm^{-3})
$\delta n_p, \delta p_n$	Excess minority carrier electron and excess minority carrier hole concentration (cm^{-3})
ϵ	Permittivity (F/cm^2)
ϵ_0	Permittivity of free space (F/cm^2)
ϵ_{ox}	Permittivity of an oxide (F/cm^2)
ϵ_r	Relative permittivity or dielectric constant
ϵ_s	Permittivity of a semiconductor (F/cm^2)
λ	Wavelength (cm or μm)
μ	Permeability (H/cm)
μ'	Ambipolar mobility (cm^2/V-s)
μ_n, μ_p	Electron and hole mobility (cm^2/V-s)

μ_0	Permeability of free space (H/cm)
ν	Frequency (Hz)
ρ	Resistivity (Ω-cm), volume charge density (C/cm^3)
σ	Conductivity (Ω^{-1} cm^{-1})
$\Delta\sigma$	Photoconductivity (Ω^{-1} cm^{-1})
σ_i	Intrinsic conductivity (Ω^{-1} cm^{-1})
σ_n, σ_p	Conductivity of n-type and p-type semiconductor (Ω^{-1} cm^{-1})
τ	Lifetime (s)
τ_n, τ_p	Electron and hole lifetime (s)
τ_{n0}, τ_{p0}	Excess minority carrier electron and hole lifetime (s)
τ_0	Lifetime in space charge region (s)
ϕ	Potential (volt)
$\phi(t)$	Time-dependent wave function
$\Delta\phi$	Schottky barrier lowering potential (volt)
ϕ_{Bn}	Schottky barrier height (volt)
ϕ_{B0}	Ideal Schottky barrier height (volt)
ϕ_{fn}, ϕ_{fp}	Potential difference (magnitude) between E_{Fi} and E_F in n-type and p-type semiconductor (volt)
ϕ_{Fn}, ϕ_{Fp}	Potential difference (with sign) between E_{Fi} and E_F in n-type and p-type semiconductor (volt)
ϕ_m	Metal work function (volt)
ϕ'_m	Modified metal work function (volt)
ϕ_{ms}	Metal-semiconductor work function difference (volt)
ϕ_n, ϕ_p	Potential difference (magnitude) between E_c and E_F in n-type and between E_v and E_F in p-type semiconductor (volt)
ϕ_s	Semiconductor work function (volt), surface potential (volt)
χ	Electron affinity (volt)
χ'	Modified electron affinity (volt)
$\psi(x)$	Time-independent wave function
ω	Radian frequency (s^{-1})
Γ	Reflection coefficient
E	Electric field (V/cm)
E_H	Hall electric field (V/cm)
$\mathrm{E}_{\mathrm{crit}}$	Critical electric field at breakdown (V/cm)
$\Theta(\theta)$	Angular wave function
Φ	Photon flux (cm^{-2} s^{-1})
$\Phi(\phi)$	Angular wave function
$\Psi(x, t)$	Total wave function

EXHIBIT A-5

United States Patent [19]
Morin et al.

[11] **4,343,081**
[45] **Aug. 10, 1982**

[54] **PROCESS FOR MAKING SEMI-CONDUCTOR DEVICES**

[75] Inventors: **Francois Morin,** Lanmerin; **Madeleine Bonnel,** Lannion, both of France

[73] Assignee: **L'Etat Francais represente par le Secretaire d'Etat aux Postes et Telecommunications et a la Telediffusion (Centre National d'Etudes des Telecommunications),** Issy les Moulineaux, France

[21] Appl. No.: **160,213**

[22] Filed: **Jun. 17, 1980**

[30] **Foreign Application Priority Data**

Jun. 22, 1979 [FR] France 79 16083
Dec. 18, 1979 [FR] France 79 30954

[51] **Int. Cl.**^{3} **H01L 21/225**
[52] **U.S. Cl.** **29/571;** 148/187; 148/188
[58] **Field of Search** 29/571; 357/23; 148/174, 188, 187

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Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—Pearne, Gordon, Sessions, McCoy & Granger

[57] **ABSTRACT**

The present invention relates to a process for making semi-conductor components on an amorphous substrate, comprising two phases, wherein, in a first phase, the substrate is introduced into a deposition chamber and a uniform deposit is made of four successive primary layers on all this substrate, without contact with the outside atmosphere: a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal; and, in a second phase, the substrate coated with these four layers is withdrawn from the deposition chamber and the last three layers are subjected to photoetching and ancillary deposition operations, which are appropriate for the structure of the component to be obtained.

5 Claims, 11 Drawing Figures

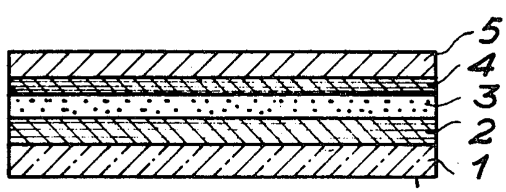
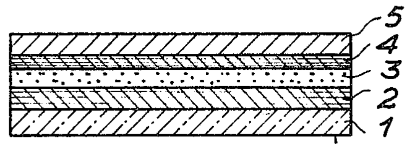


FIG.1



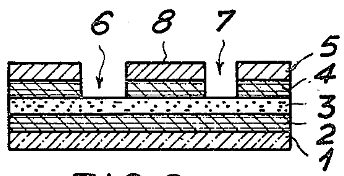


FIG.2a

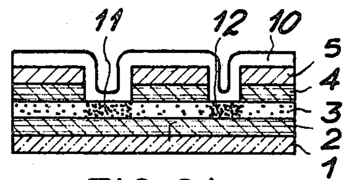


FIG.2b

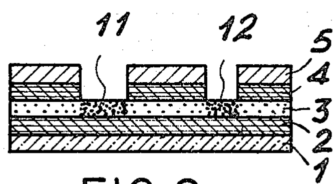


FIG.2c

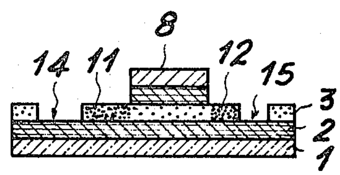


FIG.2d

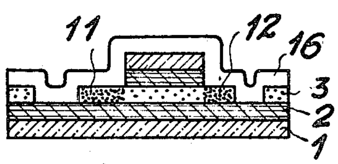


FIG.2e

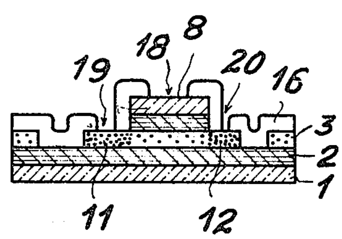


FIG.2f

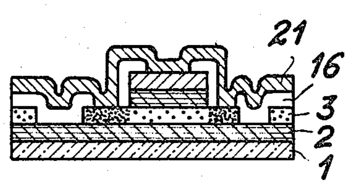


FIG.2g

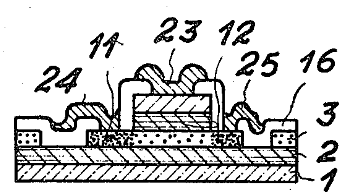


FIG.2h

FIG.3

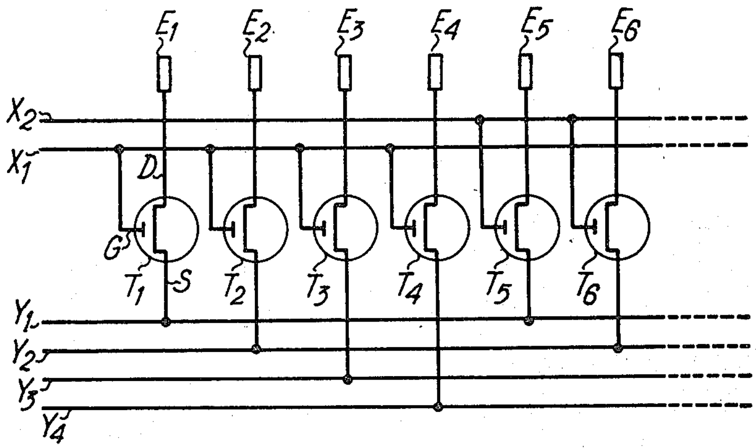

E1
E2
E3
E4
E5
E6
X2
X1
D
G
S
T1
T2
T3
T4
T5
T6
Y1
Y2
Y3
Y4

FIG.4

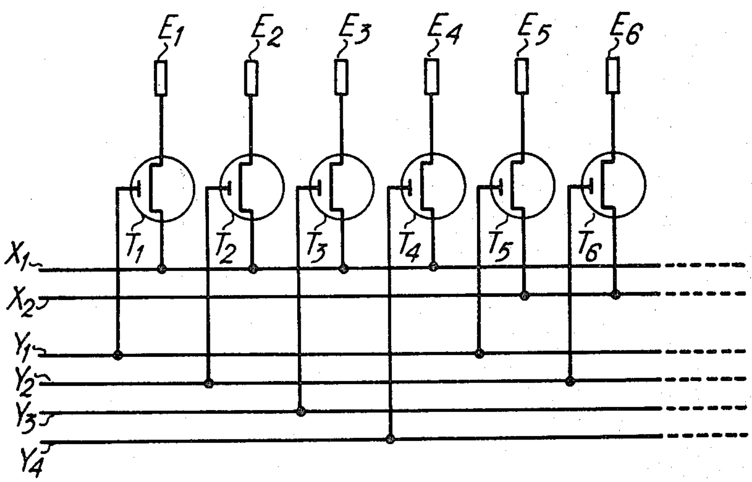

E1
E2
E3
E4
E5
E6
T1
T2
T3
T4
T5
T6
X1
X2
Y1
Y2
Y3
Y4

FIG.5a

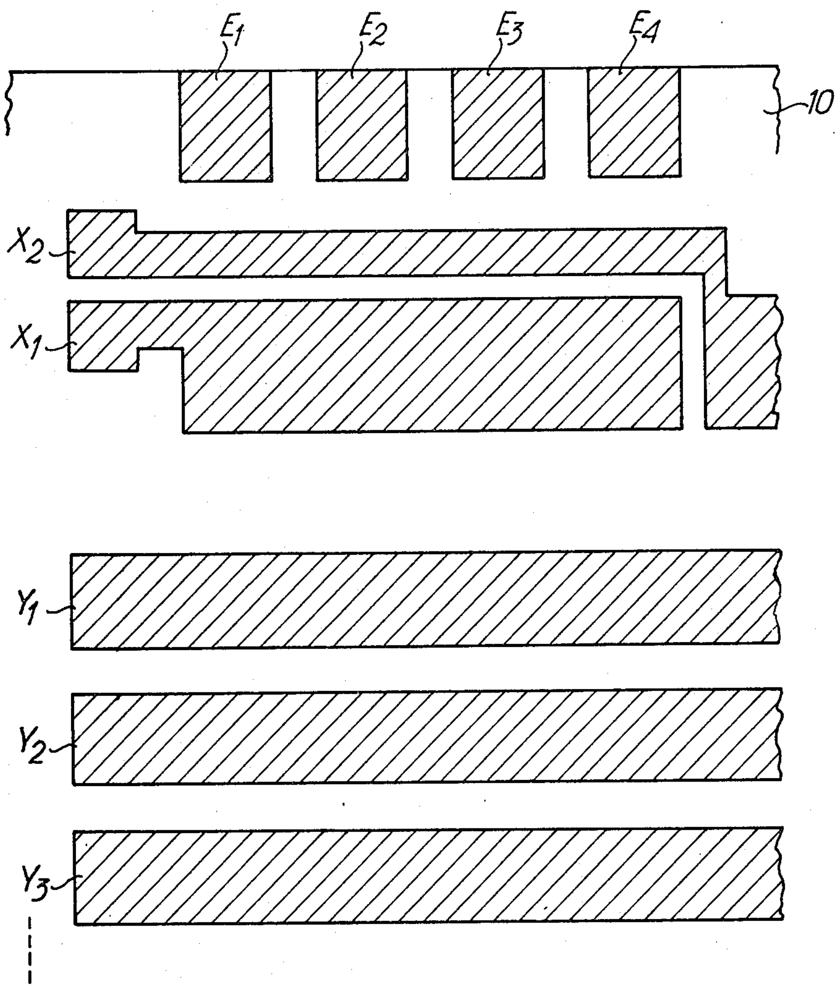


FIG. 5b

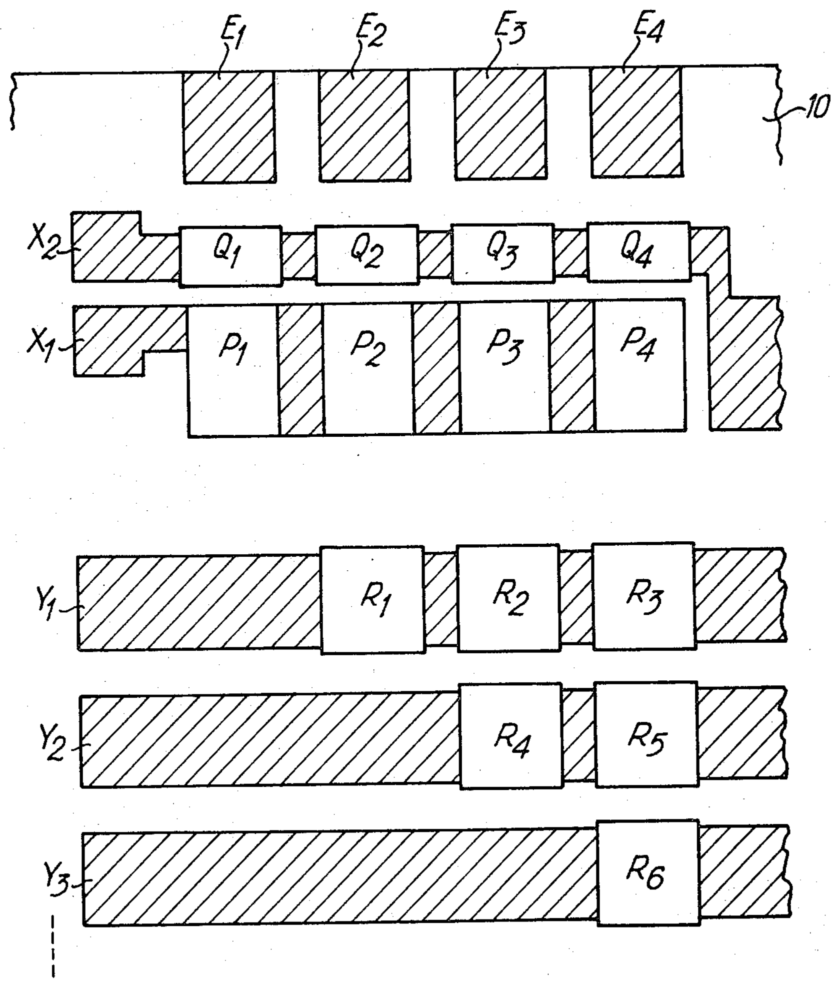


FIG.5c

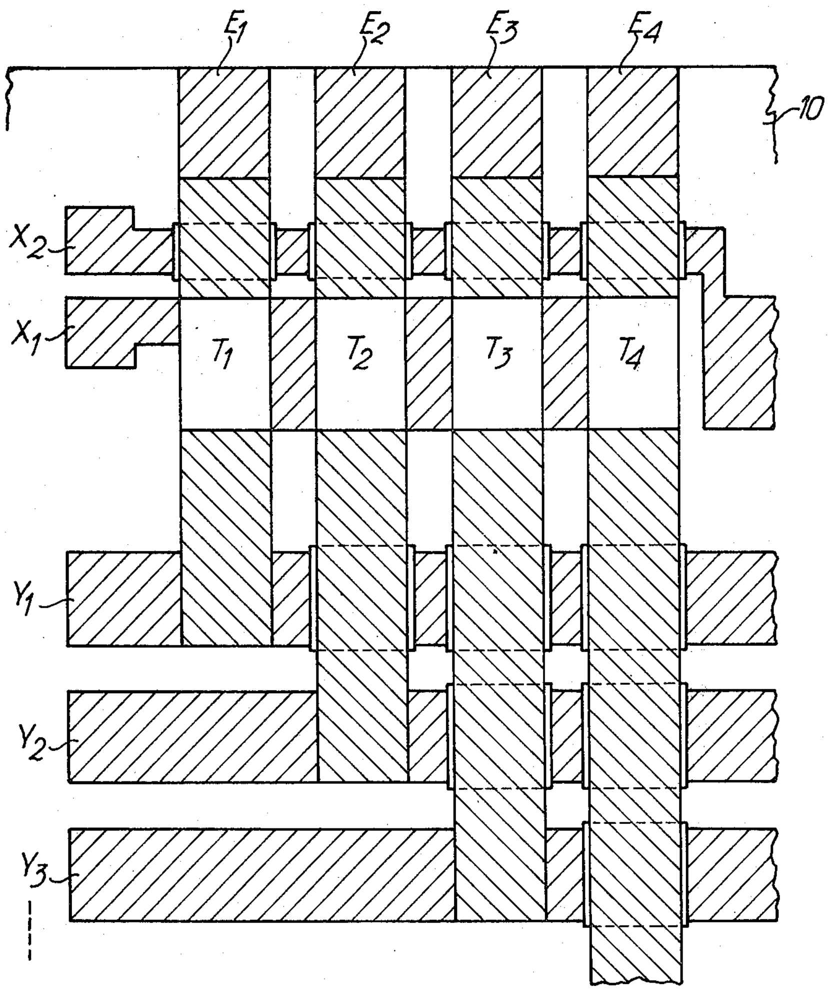


FIG. 6a

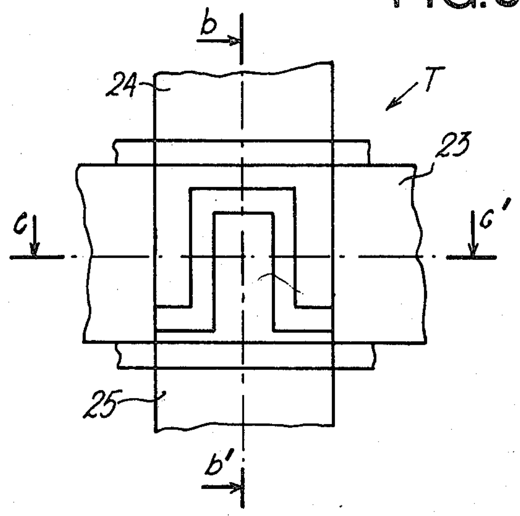


FIG. 6b

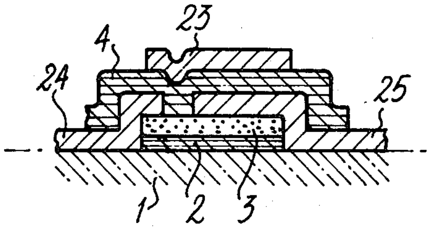


FIG. 6c

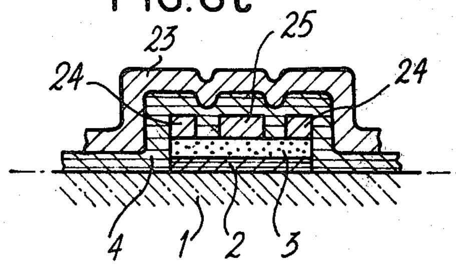
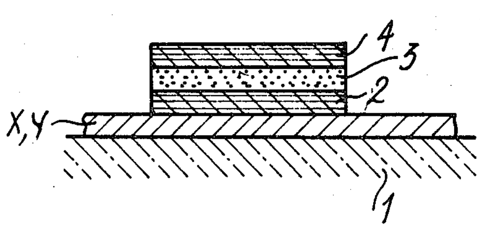


FIG. 7



PROCESS FOR MAKING SEMI-CONDUCTOR DEVICES

The present invention relates to a process for making semi-conductor components and to a component obtained by this process. It finds particular application in the production of thin-film transistors (hereinafter abbreviated to T.F.T.s) and of circuits using T.F.T.s.

A T.F.T. is a field effect transistor with insulated grid. It is similar to an MOS (metal-oxide semiconductor) transistor, with the difference that it is made on an amorphous substrate and not on a monocrystalline silicon wafer. Consequently, T.F.T. circuits may be of very large dimensions and are no longer limited by the size of the crystalline substrate.

In practice, a T.F.T. is obtained by deposit in vacuo of its different constituents on a glass substrate. Each layer (semiconductor, insulator, metal) is deposited through a metal mask (of the Stencil-mask type) in intimate contact with the substrate. To have a good definition of the patterns, the deposits are made by evaporation in vacuo. The materials to be evaporated are disposed in crucibles heated by the Joule effect or by electron bombardment. The in-situ masking excludes deposits in a gaseous atmosphere (cathode sputtering, chemical deposit by gaseous process, etc.) because of the sheath phenomena which render the edges of the patterns blurred. In the best of cases, an in vacuo mask exchanger enables all the T.F.T. (or T.F.T. circuit) to be made in one pumping cycle, this avoiding pollution of the semiconducting layer and of the insulator-semiconductor interface.

Concerning this technique and applications thereof, the article by A. G. Fischer entitled 'Flat TV panels with polycrystaline layers' published in the journal 'Microelectronics', Vol. 7, No. 4, 1976, pages 5 to 15, may be consulted.

Although the main advantage of this technique of making T.F.T.s is a rapid execution of the circuits, it has the drawback of being suitable only for circuits of modest dimensions and definition. In fact, a metal mask of high definition and large outer dimensions comprises a large number of very small openings, has mediocre mechanical properties, expands, and deforms. As a plurality of masks are necessary and as the patterns must be superimposed with high precision, a limitation is rapidly apparent. It is estimated that this method enables circuits of overall dimensions of the order of about ten centimeters to be produced, not having more than four transistors per square millimeter. These modest performances limit the applications of the T.F.T.

Furthermore, this technique imposes that the layers constituting the transistor be disposed on a substrate at ambient temperature, in order to avoid the expansion of the masks. Now, the semiconductor deposit which is generally polycrystalline, would necessitate the use of a much higher substrate temperature (a few hundred degrees) in order to improve crystallization.

Other processes of manufacture have been developed, employing partial photoetching of the layers. They have the drawback of polluting the semiconductor layer in its active part. A description of these processes will be found in the article by J. C. Erskine and A. Cserhati entitled 'Cadmium selenide thin-film transistors' published in the journal 'Journal of Vaccum Science Technology', Vol. 15(6), Nov./Dec. 1978, pages 1823 to 1835.

It is an object of the present invention to provide a process for manufacturing semiconductor components and particularly T.F.T.s, which avoids all these drawbacks. The process of the invention employs the principle of photoetching whilst conserving one of the advantages of the process described hereinabove, namely the production of all the layers constituting the T.F.T. in one manufacturing cycle, thus avoiding the pollution of the layers and interfaces by outside agents. However, the invention has the following advantages over the known process:

1. The substrate may be heated during the deposit of the semiconductor, this leading to an improvement in the crystallization.

2. The dimensions of the substrate may be as large as is desired, within the limit of the homogeneity of the deposits.

3. The deposition techniques are no longer limited to evaporation is vacuo and cathode sputtering, chemical deposit by gas process, etc. may be used.

4. The definition of the patterns is increased by the use of photographic masks of high precision, already used for making integrated circuits.

5. The complexity of the circuits made is greater and attains that of integrated circuits.

6. The process of photoetching described hereinbelow effects the self-alignment of the grid on the channel of the T.F.T., this eliminating the parasitic grid-source and grid-drain capacitances.

To this end, the process according to the invention comprises two phases:

(A) in a first phase,

- the substrate is introduced into a deposition chamber,
- a uniform deposit of four successive primary layers is made on all this substrate, without contact with the outside atmosphere: a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

(B) and, in a second phase:

- the substrate coated with these four layers is withdrawn from the deposition chamber,
- the last three layers are subjected to photoetching and ancillary deposition operations, which are appropriate for the structure of the component to be obtained.

The invention will be more readily understood on reading the following description with reference to the accompanying drawings, in which:

FIG. **1** shows a schematic section of the substrate obtained after the first phase,

FIG. **2** shows a schematic section of the structure obtained at various stages of the second phase,

FIG. **3** schematically shows a multiplexed T.F.T. control circuit for a teleprinter restitution head, according to a first embodiment,

FIG. **4** schematically shows a multiplexed T.F.T. control circuit for a teleprinter restitution head, according to a second embodiment,

FIGS. **5***a*, **5***b* and **5***c* schematically show, in plan view, three stages of manufacture of the control circuit,

FIG. **6** shows a T.F.T. in plan view (a) and in transverse sections (b) and (c).

FIG. **7** shows a crossing zone in section.

Referring now to the drawings, FIG. **1** shows in schematic section (neither the proportion nor the dimensions are respected) a substrate **1** on which are

deposited; a thick layer **2** of insulating material, a layer **3** of semiconductor, a thin layer **4** of insulator and finally a layer **5** of metal. The operating conditions relative to this first phase may be as follows:

The substrate **1** on which it is desired to make the T.F.T. circuit is firstly introduced into a deposition chamber. Four successive deposits are made, without contact with the outside atmosphere:

1. Deposit of the thick insulating layer **2**

To protect the circuit from the impurities which may be contained in the substrate, a thick insulating layer **2** is firstly deposited, after degassing. This layer will serve as barrier for the alkaline ions which might diffuse in the semiconductor and deteriorate it. A layer of alumina deposited by evaporation of sapphire employing an electron gun may for example be used.

2. Deposit of the semiconductor film **3**

For this operation, the substrate is taken to as high a temperature as possible (generally a little below 500° C. if the substrate is made of glass). In the example described here, the semiconductor is cadmium selenide—CdSe—deposited by evaporation in vacuo. The temperature of the substrate is maintained at 400° C. during the deposition.

3. Deposit of the thin insulating layer **4**

The grid insulator is then deposited. The power of modulation of the grid depends on its dielectric qualities. Its thickness will determine the breakdown voltage of the transistor. In the example described here, a thin layer of alumina, prepared as in **1**, is used.

4. Deposit of the grid metal **5**

Molybdenum evaporated with an electron gun may be used.

At this stage, the deposits may undergo an appropriate thermal treatment: annealing in vacuo or in a special atmosphere.

After it has been removed from the deposition chamber, the substrate, on which the four primary layers have just been deposited, is then subjected to the operations of photoetching and ancillary deposits appropriate for the second phase.

Photoetching consists in using a photosensitive resin, sensitized to ultra-violet light, through a photographic mask reproducing the desired pattern. After development and hardening of the resin, the exposed parts are eliminated by chemical etching. After etching, the protective layer of resin may easily be removed by dissolution in a suitable solvent.

This technique is currently used in the manufacture of integrated circuits and transistors, but, in the present case, the steps of the process of manufacture are different and original. They are illustrated in FIG. 2, which shows eight sections a, b, c, d, e, f, g, and h, corresponding to the following eight phases:

(a) Photoetching of the metal layer **5** and the insulating layer **4** with the aid of a first mask. This first photoetching makes windows **6** and **7** on the semiconductor and defines the grids **8** of the T.F.T.s. In the example described here, the molybdenum and alumina not protected by the resin are selectively attacked by immersion in acid solutions.

(b) Deposit of a diffusing metal **10** and diffusion thereof by annealing. This diffusion renders the parts **11** and **12** of the semiconductor **3** defined in (a) conducting; the diffusing metal may be aluminum or chromium, and may diffuse towards 400° C.

(c) Elimination of the excess metal by chemical attack, which must be selective, since it must leave the grid metal **5** intact.

(d) With the aid of a second mask, photoetching of the semiconductor layer in order to create windows **14** and **15** which insulate the components on the substrate. In the example taken, the cadmium selenide may be eliminated by a solution of bromine-ethanol.

(e) Deposit of a thick insulator **16**, different from insulators **1** and **4**. This may, for example, be SiO_2.

(f) With the aid of a third mask and a selective chemical attack, opening of windows **18**, **19** and **20** in the thick insulator, in order to be able to make contacts on the grid **8**, source **11** and drain **12** of each transistor.

(g) Deposit of a layer **21** of contact metal. This metal may, for example, be aluminum.

(h) With the aid of a fourth mask, photoetching of the contacts. Contact **23** of the grid, **24** of the source and **25** of the drain are then obtained.

The process of manufacture which has just been described, by the advantages that it procures, extends the field of application of the T.F.T. The possibility of making circuits of large dimensions (the limit is imposed by the homogeneity of the deposits and the capacity of the mask aligner, but the production of circuits of several square decimeters may be envisaged) enables circuits to be designed for controlling flat screens, directly on the support of the screen, this solving the problems of connection. The high resolution of the photoetching allows the production of complex circuits (shift register, memories, multiplexing circuits, etc.) and makes it possible to make circuits associated with display matrices or teleprinter heads (read-out/restitution).

A process for making a restitution head for a teleprinter will be described by way of example.

It will be recalled that the electrosensitive paper which may be used in teleprinting may be classified in two families, the first grouping electrothermosensitive and metallized papers, and second grouping the electrolytic and electrocatalytic ones.

At the present time, only slow teleprinters (employing stylet) or alphanumerical printers are known for the first family; for the second family, no marketed apparatus exists.

To obtain a rapid teleprinter, of the same type as those which use (or which will use) heat-sensitive paper, a restitution head with multiple electrodes disposed in the form of a comb must be produced so that the mechanical displacements of the head are eliminated. There is then a problem of connection due to the very large number of connecting wires emerging from the head and the high definition of the electrodes, hence the necessity of multiplexing the latter. According to a known art, this multiplexing is obtained by associating a diode with each electrode.

Now, if, instead of heat-sensitive paper, an electrosensitive paper is used having a conducting base, the multiplexing circuits with diodes become unsuitable. It is no longer a diode which must be associated with each electrode, but a transistor, this considerably increasing the problems of connection.

It is an object of the present invention to solve this problem. To this end, the process used is characterized in that:

a row of electrodes (E_1, E_2 . . .) and two families of metal multiplexing channels (X_1, X_2 . . . and Y_1, Y_2 . . .

) parallel to one another and to said row, are deposited on an insulating substrate;

four primary layers, insulating, semiconducting, insulating and metallic, respectively, are deposited on this substrate by the operations of the first phase mentioned hereinbefore;

the operations of the second phase, are then effected, the photoetching operations being carried out so as to leave zones constituted by said four layers, these zones being disposed on the one hand opposite each electrode at the desired site for control transistors (zones P_1, P_2 . . .) and on the other hand at crossing sites located on the two families of metal channels on a level with the electrodes (zones Q_1, Q_2 . . . on the first family and R_1, R_2 . . . on the second);

the operations in accordance with those described hereinabove are carried out on zones P_1, P_2 . . . to obtain at each site a T.F.T., or T_1, T_2 . . .

during the operations of depositing the layer of contact metal of the T.F.T.s and of photoetching this layer, metal connecting channels are produced, connecting, for each T.F.T., the grid to one of the multiplexing channels of one of the families, the source to one of the channels of the other family and the drain to the electrode disposed opposite this T.F.T.

The restitution head shown in FIGS. **3** and **4**, in two slightly different embodiments, comprises read-in electrodes E_1, E_2 . . . connected to transistors T_1, T_2 . . . of T.F.T. type. Each of these transistors comprises a grid G, a source S and a drain D. The control circuit of these transistors comprises two families of metal channels the first formed by channels X_1, X_2 . . . and the second of channels Y_1, Y_2 . . . In the variant of FIG. **3**, the channels X_1, X_2 . . . are connected to the grids of the T.F.T.s and the channels Y_1, Y_2 . . . to the sources of said T.F.T.s. In the variant of FIG. **4**, the channels X_1, X_2 . . . are connected to the sources of the T.F.T.s and the channels Y_1, Y_2 . . . to the grids of said T.F.T.s.

The principle of functioning of these two variants of a restitution head is summarized in the two Tables I and II hereinafter, in which a "1" indicates the application of a control voltage to a channel and a "0" the absence of such a voltage. In these Tables, only a few electrodes are shown in the first column, the others being controlled in accordance with the same principle.

FIGS. **5***a* to **5***c* illustrate different steps of the process for manufacturing a restitution head according to the variant of FIG. **3**.

Electrodes E_1, E_2 . . . and metal multiplexing channels X_1, X_2 . . . and Y_1, Y_2, Y_3 . . . are deposited on an insulating substrate **10** (for example made of glass). This deposit may be effected by evaporation in vacuo using an electron gun. The material to be evaporated is, for example, gold deposited on a chromium adhering layer. The shape of the electrodes and channels is obtained by photoetching. The substrate then has the appearance of FIG. **5***a* where the dimensions and proportions have not been respected in order to render the drawing clearer. The contact studs and supply circuits have not been shown.

Four consecutive deposits (insulator/semiconductor/insulator/metal) are then made on the whole substrate of FIG. **5***a*, in accordance with the technique described hereinbove.

A first photoetching of these layers is carried out so as to leave zones P_1, P_2, P_3 . . . at the site of the future T.F.T.s and zones Q_1, Q_2, Q_3 . . . on channels X_1, X_2 . . . level with the electrodes, and finally, zones R_1, R_2, R_3 . . . on channels Y_1, Y_2 . . . at the site of the future crossings on the multiplexing channels (FIG. **5***b*).

Transistors T_1, T_2, T_3 . . . are then made at the site of zones P_1, P_2, P_3 . . . , in accordance with the operations described hereinbefore (FIG. **5***c*).

In FIG. **6**, a transistor T is shown in plan view (a) and in section along bb' and along cc' (b and c respectively). The references used in this Figure are those of FIG. **1**: substrate **1**, first insulating layer **2**, semiconductor layer **3**, second insulating layer **4**, grid contact **23**, source contact **24**, and drain contact **25**.

The crossing zones Q_1, Q_2 . . . and R_1, R_2 . . . are intended to avoid the electrical contacts between the vertical connections and the horizontal multiplexing channels. Of course, these channels do not exist at the site where a multiplexing channel must be connected to a vertical connection. A crossing zone comprises, in accordance with FIG. **7**, on one of the conducting channels X or Y deposited on the substrate, three of the four layers deposited during the first phase, namely an insulating layer **2**, a semiconductor layer **3** and an insulating layer **4**. The upper metal layer **5** of the zones is eliminated at the moment of photoetching of the grid of the T.F.T.s. This therefore does not involve any additional operation. Of course, the semiconducting properties of the layer **3** play no role in this insulation structure.

The crossing zones advantageously have dimensions which slightly exceed the dimensions of the conducting channels which they are to insulate.

The connections between the transistors, the restitution electrodes and the appropriate control channels are obtained by deposits of metal layers made during the deposit of the metal layer intended for producing the contacts of the T.F.T.s (reference **21** in FIG. **2***g*) The final result is illustrated in FIG. **5***c*.

Thus, apart from the prior deposit of the multiplexing channels, the process for manufacturing the control circuit according to the ivention merely uses operations necessary for obtaining T.F.T.s and therefore does not involve any additional operation.

TABLE I

Electrodes	Control					
	X_1	X_2	Y_1	Y_2	Y_3	Y_4
E_1	1	0	0	1	1	1
E_2	1	0	1	0	1	1
E_5	0	1	0	1	1	1
E_6	0	1	1	0	1	1

TABLE II

Electrodes	Control					
	X_1	X_2	Y_1	Y_2	Y_3	Y_4
E_1	0	1	1	0	0	0
E_2	0	1	0	1	0	0
E_5	1	0	1	0	0	0
E_6	1	0	0	1	0	0

What is claimed is:

1. In a process for making thin film transistors on an amorphous substrate, the steps;

(A) in a first phase: of introducing the substrate in a deposition chamber, making on all this substrate, without contact with the outside atmosphere, a uniform deposit of four successive primary layers; a first layer of protective insulating material, a second layer of semiconductor material, a third

layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

(B) and, in a second phase,

of withdrawing the substrate coated with these four layers from the deposition chamber, by a first photoetching operation through a first mask, two openings for each transistor are opened through the fourth layer of metal and the third layer of insulator, the metal part remaining between these two openings constituting the grid of the transistor, and

a layer of diffusing metal is deposited on the whole of the substrate, then, by selective chemical attack, this second metal is eliminated, this leaving, in the semiconductor, two conducting zones, one constituting the drain and the other the source of the transistor.

2. The process of claim **1**, wherein, with the aid of a second mask, a photoetching is then effected of the semiconductor in order to separate the transistors from one another.

3. The process of claim **2**, wherein a deposit of a thick insulator different from the insulator used for the first and the third layer is then made on the whole substrate, after which, with the aid of a third mask, a window is opened in this thick insulator opposite the grid, the drain and the source.

4. The process of claim **3**, wherein a deposit is then made of a layer of contact metal on the whole substrate after which, with the aid of a fourth mask, this layer is photoetched in order to obtain a grid contact, a drain contact and a source contact.

5. A process for making a restitution head of a teleprinter comprising a row of electrodes connected to a multiplexed control circuit, comprising the steps of:

depositing on an insulating substrate a row of electrodes and two families of metal multiplexing channels parallel to one another and to said row,

making on all this substrate, without contact with the outside atmosphere, a uniform deposit of four successive primary layers; a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

carrying out a photoetching operation being so as to leave zones constituted by said four layers, these zones being disposed on the one hand opposite each electrode at the desired site for control resistors and on the other hand at crossing sites located on the two families of metal channels on a level with the electrodes,

carrying out on said zones operations to obtain at each site a thin film transistor, these operations consisting in a first photoetching operation through a first mask, two openings for each transistor being opened through the fourth layer of metal and the third layer of insulator, the metal part remaining between these two openings constituting the grid of the transistor and in depositing a layer of diffusing metal on the whole of the substrate, then in selective chemical attacking of this metal for eliminating it, this leaving, in the semiconductor, two conducting zones, one constituting the drain and the other the source of the transistor, and

during the operations of depositing the layer diffusing metal layer of the thin film transistors, and of photoetching this layer, producing metal connecting channels connecting, for each transistor, the gate to one of the multiplexing channels of one of the families, the source to one of the channels of the other family and the drain to the electrode disposed opposite this transistor.

* * * * *

EXHIBIT A-6

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use of the metric system. Today, most of the dimensions are specified using the metric system, although Imperial units are occasionally still used. Throughout the rest of this book, we will attempt to make consistent use of metric units.

1.2 AN OVERVIEW OF MONOLITHIC FABRICATION PROCESSES AND STRUCTURES

Monolithic IC fabrication can be illustrated by studying the basic cross sections of MOS and bipolar transistors in Figs. 1.4 (on page 7) and 1.5 (on page 8). The n-channel MOS transistor is formed in a p-type substrate. Source/drain regions are formed by selectively converting shallow regions at the surface to n-type material. Thin and thick silicon-dioxide regions on the surface form the gate insulator of the transistor and serve to isolate one device from another. A thin film of polysilicon is used to form the gate of the transistor, and a metal such as aluminum is used to make contact to the source and drain. Interconnections between devices can be made using the diffusions and the layers of polysilicon and metal.

The bipolar transistor in Fig. 1.5 has alternating n- and p-type regions selectively fabricated on a p-type substrate. Silicon dioxide is again used as an insulator, and aluminum is used to make electrical contact to the emitter, base, and collector of the transistor.

Both the MOS and bipolar structures are fabricated through the repeated application of a number of basic processing steps:

- Oxidation
- Photolithography
- Etching
- Diffusion
- Evaporation or sputtering
- Chemical vapor deposition (CVD)
- Ion implantation
- Epitaxy
- Annealing

Silicon dioxide can be formed by heating a silicon wafer to a high temperature (1000 to 1200 °C) in the presence of oxygen. This process is called *oxidation*. Metal films can be deposited through evaporation by heating the metal to its melting point in a vacuum. Thin films of silicon nitride, silicon dioxide, polysilicon, and metals can all be formed through a process known as *chemical vapor deposition* (CVD), in which the material is deposited out of a gaseous mixture onto the surface of the wafer. Metals and insulators may also be deposited by a process called *sputtering*.

Shallow n- and p-type layers are formed by high-temperature (1000 to 1200 °C) *diffusion* of donor or acceptor impurities into silicon or by *ion implantation*, in which the wafer is bombarded with high-energy donor or acceptor ions generated in a high-voltage particle accelerator.

In order to build devices and circuits, the n- and p-type regions must be formed selectively in the surface of the wafer. Silicon dioxide, silicon nitride, polysilicon, photo resist, and other materials can all be used to mask areas of the wafer surface to prevent

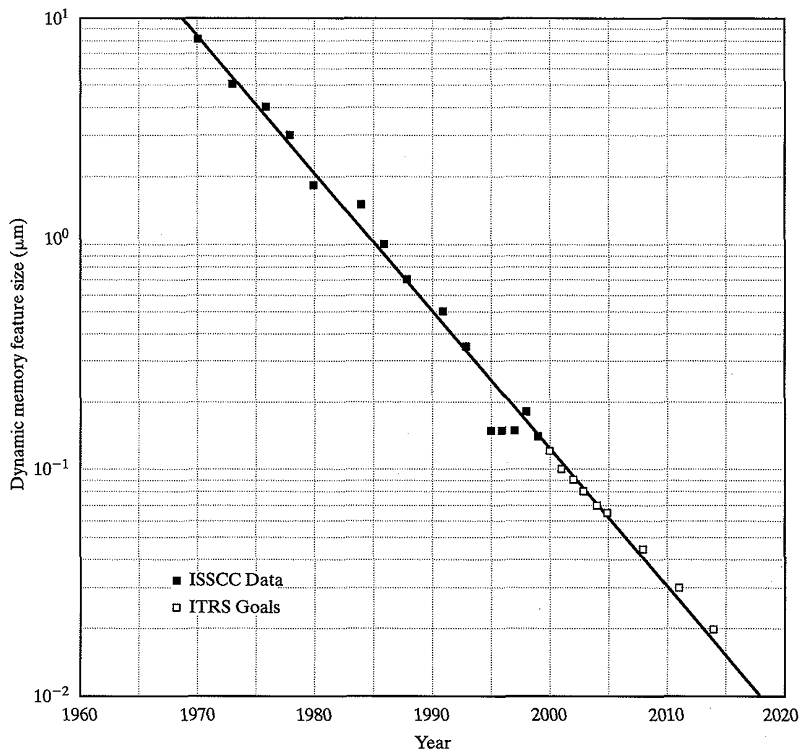

FIGURE 1.3
Feature size used in fabrication of dynamic memory as a function of time.

TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

	Selected Projections					
Year of First Product Shipment	2001	2003	2005	2008	2011	2014
DRAM Metal Line Half-Pitch (nm)	150	120	100	70	50	35
Microprocessor Gate Widths (nm)	100	80	65	45	30	20
DRAM (G-bits/chip)	2.2	4.3	8.6	24	68	190
Microprocessor (M-transistors/chip)	48	95	190	540	1500	4300
DRAM Chip Area: Year of Introduction (mm^2)	400	480	526	600	690	790
DRAM Chip Area: Production (mm^2)	130	160	170	200	230	260
MPU Chip Size at Introduction (mm^2)	340	370	400	470	540	620
MPU Chip Area: Second "shrink" (mm^2)	180	210	230	270	310	350
Wafer Size (mm)	300	300	300	450	450	450

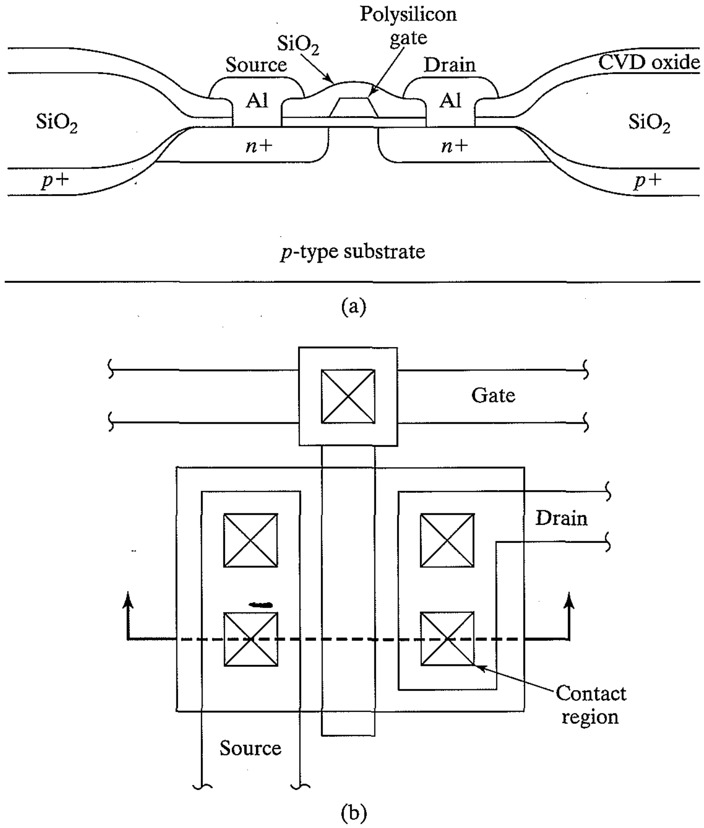

FIGURE 1.4
The basic structure of an n-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate "metal."

penetration of impurities during ion implantation or diffusion. Windows are cut in the masking material by etching with acids or in a plasma. Window patterns are transferred to the wafer surface from a mask through the use of optical techniques. The masks are also produced using photographic reduction techniques.

Photolithography includes the overall process of mask fabrication, as well as the process of transferring patterns from the masks to the surface of the wafer. The photolithographic process is critical to the production of integrated circuits, and the number of mask steps is often used as a measure of complexity when comparing fabrication processes.

1.3 METAL-OXIDE-SEMICONDUCTOR (MOS) PROCESSES

1.3.1 Basic NMOS Process

A possible process flow for a basic n-channel MOS process (NMOS) is shown in Fig. 1.6 on page 9 and Fig. 1.7 on page 10. The starting wafer is first oxidized to form a thin-pad oxide layer of silicon dioxide (SiO_2) that protects the silicon surface. Silicon nitride is then deposited by a low-pressure chemical vapor deposition (LPCVD) process. Mask #1 defines the active transistor areas. The nitride/oxide sandwich is etched away

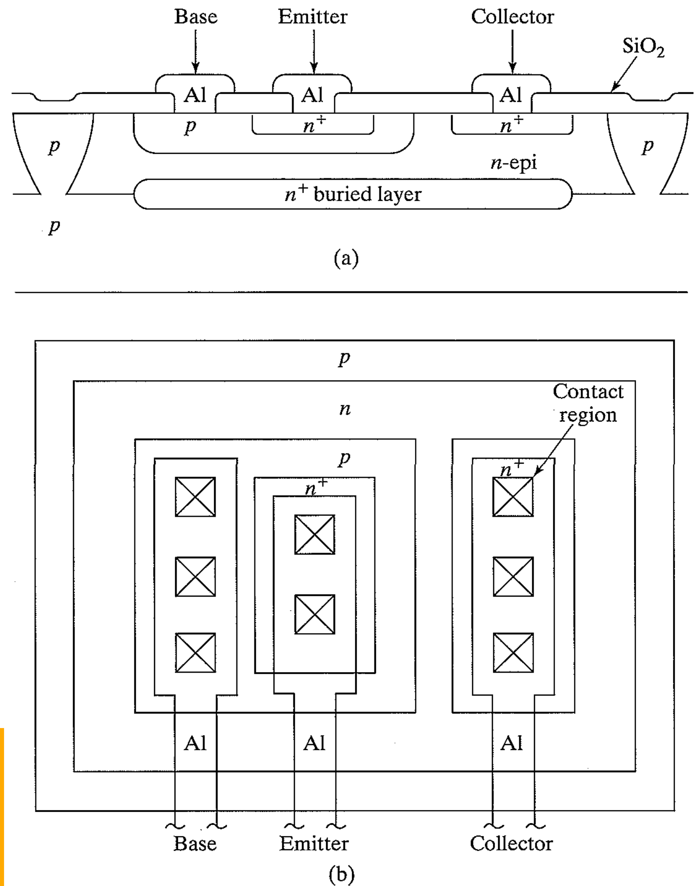

FIGURE 1.5

The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).

everywhere except where transistors are to be formed. A boron implantation is performed and followed by an oxidation step. The nitride serves as both an implantation mask and an oxidation mask. After the nitride and thin oxide padding layers are removed, a new thin layer of oxide is grown to serve as the gate oxide for the MOS transistors. Following gate-oxide growth, a boron implantation is commonly used to adjust the threshold voltage to the desired value.

Polysilicon is deposited over the complete wafer using a CVD process. The second mask defines the polysilicon gate region of the transistor. Polysilicon is etched away everywhere except over the gate regions and the areas used for interconnection. Next, the source/drain regions are implanted through the thin oxide regions. The implanted impurity may be driven in deeper with a high-temperature diffusion step. More oxide is deposited on the surface, and contact openings are defined by the third mask step. Metal is deposited over the wafer surface by evaporation or sputtering. The fourth mask step is used to define the interconnection pattern that will be etched in the metal. A passivation layer of phosphosilicate glass or silicon nitride (not shown in Fig. 1.6) is deposited on the wafer surface, and the final mask (#5) is used to define windows so that bonding wires can be attached to pads on the periphery of the IC die.

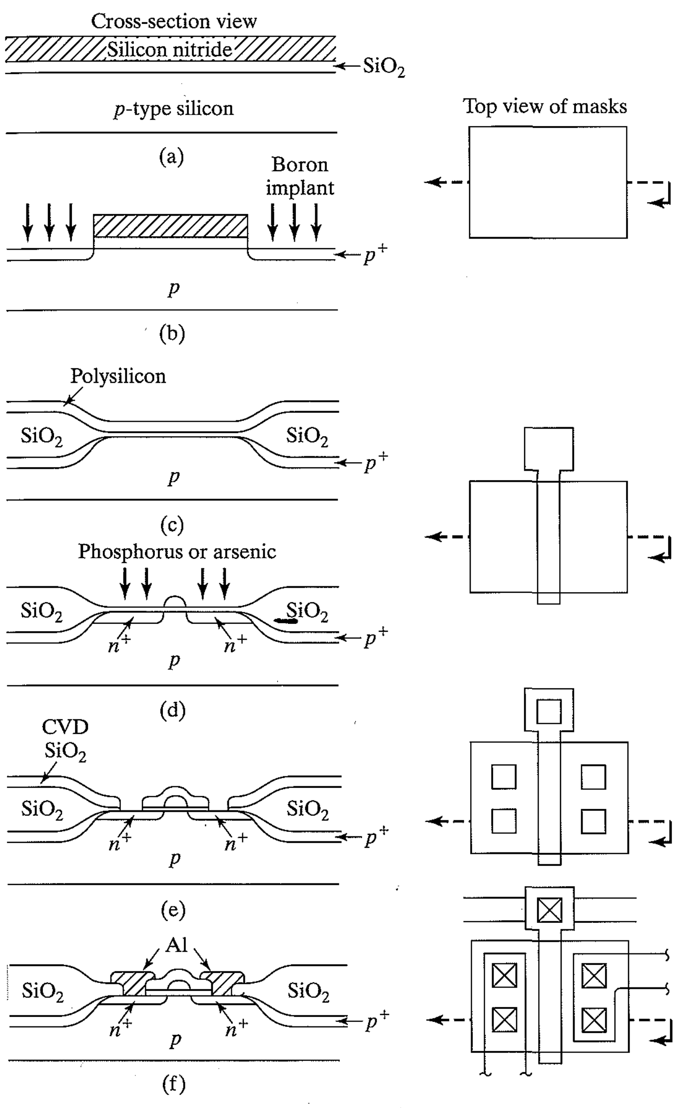

FIGURE 1.6

Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.

This simple process requires five mask steps. Note that these mask steps use subtractive processes. The entire surface of the wafer is first coated with a desired material, and then most of the material is removed by wet chemical or dry plasma etching.

1.3.2 Basic Complementary MOS (CMOS) Process

Figure 1.8 shows the mask sequence for a basic complementary MOS (CMOS) process. One new mask, beyond that of the NMOS process, is used to define the "n-well," or "n-tub," which serves as the substrate for the p-channel devices. A second new mask step is used to define the source/drain regions of the p-channel transistors.

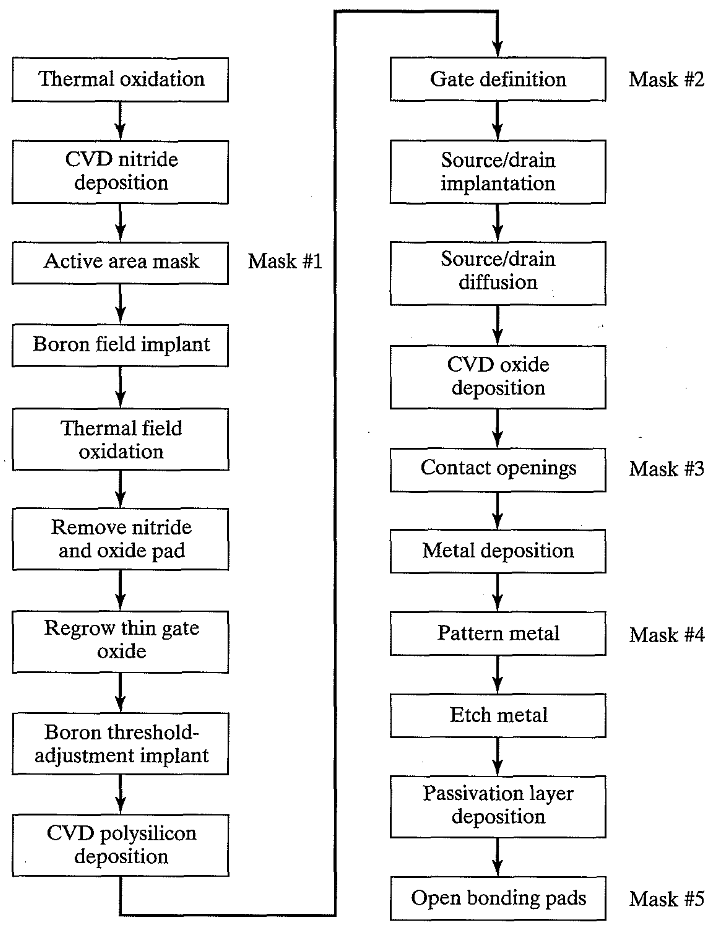

FIGURE 1.7
Basic NMOS process flowchart.

Additional masks may be used to adjust the threshold voltage of the MOS transistors and are very common in state-of-the-art NMOS and CMOS processes.

Older CMOS processes use a *p*-well instead of an *n*-well. Twin-well processes have also been developed recently. Both a *p*-well and an *n*-well are formed in a lightly doped substrate, and the *n*- and *p*-channel devices can each be optimized for highest performance. Twin-well very large-scale integration (VLSI) processes use lightly doped layers grown on heavily doped substrates to suppress a CMOS failure mode called *latchup*.

1.4 BASIC BIPOLAR PROCESSING

Basic bipolar fabrication is somewhat more complex than single-channel MOS processing, as indicated in Figs. 1.9 on page 12 and 1.10 on page 13. A *p*-type silicon wafer is oxidized, and the first mask is used to define a diffused region called the *buried layer*, or *subcollector*. This diffusion is used to reduce the collector resistance of the bipolar transistor. Following the buried-layer diffusion, a process called *epitaxy* is used to grow single-crystal *n*-type silicon on top of the silicon wafer. The epitaxial growth process results in a high-

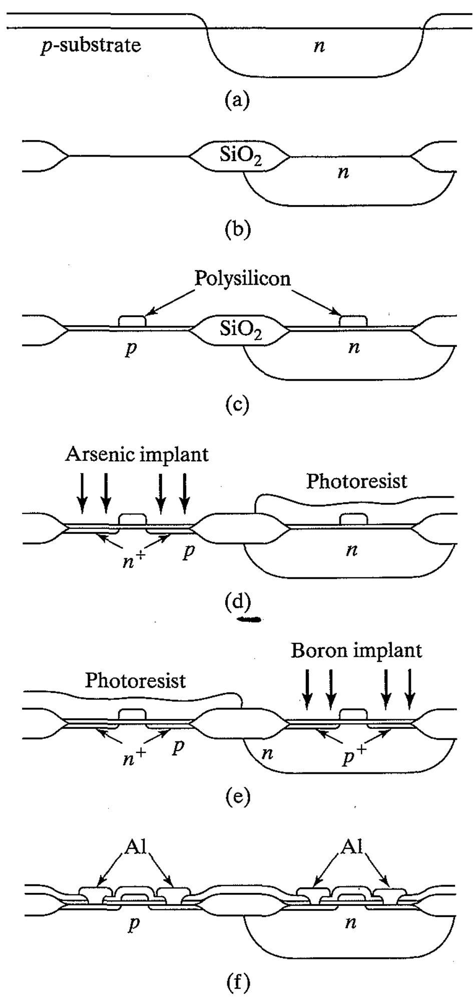

FIGURE 1.8

Cross-sectional views at major steps in a basic CMOS process. (a) Following n-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.

quality silicon layer with the same crystal structure as the original silicon wafer. An oxide layer is then grown on the wafer. Mask two is used to open windows for a deep p-diffusion, which is used to isolate one bipolar transistor from another. Another oxidation follows the isolation diffusion. Mask three opens windows in the oxide for the p-type base diffusion. The wafer is usually oxidized during the base diffusion, and mask four is used to open windows for the emitter diffusion. The same diffusion step places an n^+ region under the collector contact to ensure that a good ohmic contact will be formed during subsequent metallization. Masks five, six, and seven are used to open contact windows, pattern the metallization layer, and open windows in the passivation layer just as in the NMOS process described in Section 1.3. Thus, the basic bipolar process requires seven mask levels compared with five for the basic NMOS process.

After the MOS or bipolar process is completed, each die on the wafer is tested, and bad dice are marked with ink. The wafer is then sawed apart. Good dice are mounted in various packages for final testing and subsequent sale or use.

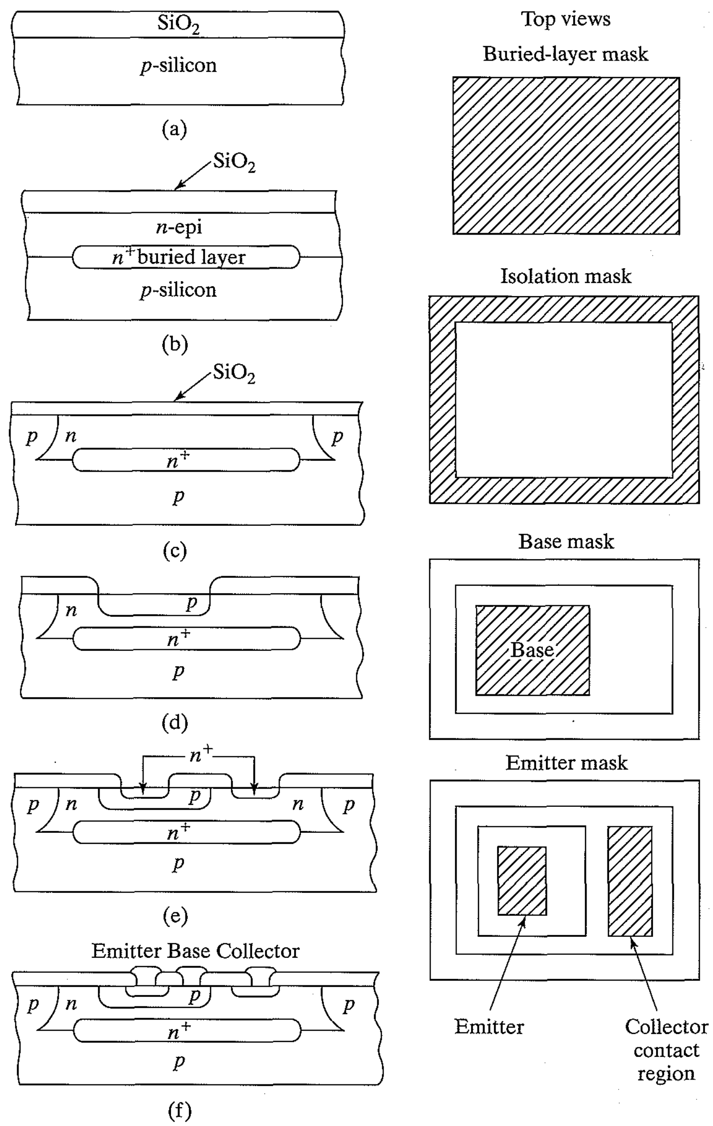

FIGURE 1.9

Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.

1.5 SAFETY

In the course of IC fabrication processes described throughout the rest of this text, we shall encounter a wide variety of acids, highly corrosive bases, organic and inorganic solvents, and materials with carcinogenic properties, as well as extremely toxic gases, and this represents a good opportunity to stress the need to exercise a high degree of caution before proceeding with any semiconductor processing. Because of the dangers, most laboratories require individuals to pass a safety test before they are permitted to work in the laboratory.

CHAPTER 2

Lithography

In order to produce an integrated circuit, thin films of various materials are used as barriers to the diffusion or implantation of impurity atoms or as insulators between conductive materials and the silicon substrate. Holes, or windows, are cut through this barrier material wherever impurity penetration or contact is desired.

Masks contain the patterns of windows that are transferred to the surface of the silicon wafer using a process called *photolithography*. Photolithography makes use of a highly refined version of the photoengraving process. The patterns are first transferred from the mask to a light-sensitive material called *photoresist*. Chemical or plasma etching is then used to transfer the pattern from the photoresist to the barrier material on the surface of the wafer. Each mask step requires successful completion of numerous processing steps, and the complexity of an IC process is often measured by the number of photographic masks used during fabrication. This chapter will explore the lithographic process, including mask fabrication, photoresist processes, and etching.

2.1 THE PHOTOLITHOGRAPHIC PROCESS

Photolithography encompasses all the steps involved in transferring a pattern from a mask to the surface of the silicon wafer. The various steps of the basic photolithographic process given in Figs. 2.1 and 2.2 will each be discussed in detail next.

Ultraclean conditions must be maintained during the lithography process. Any dust particles on the original substrate or that fall on the substrate during processing can result in defects in the final resist coating. Even if defects occur in only 10% of the chip sites at each mask step, fewer than 50% of the chips will be functional after a seven-mask process is completed. Vertical laminar-flow hoods in clean rooms are used to prevent particulate contamination throughout the fabrication process. Clean rooms use filtration to remove particles from the air and are rated by the maximum number of particles per cubic foot or cubic meter of air, as shown in Table 2.1. Clean rooms have evolved from Class 100 to the Class 1 facilities now being used for VLSI/ULSI processing. For comparison, each cubic foot of ordinary room air has several million dust particles exceeding a size of 0.5 μm.

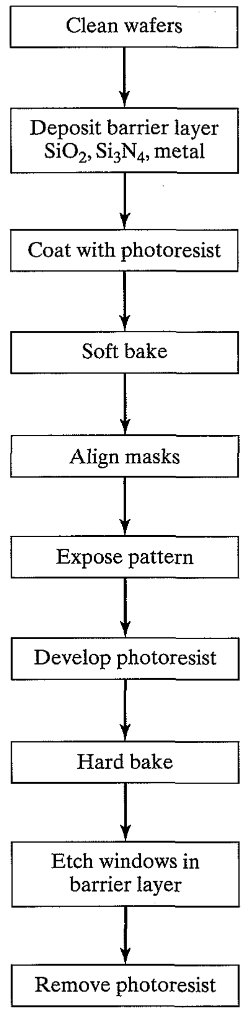

FIGURE 2.1

Steps of the photolithographic process.

TABLE 2.1 Ratings by Class of Effectiveness of Filtration in Clean Rooms

Class	Number of 0.5-μm particles per ft^3 (m^3)	Number of 5-μm particles per ft^3 (m^3)
10,000	10,000 (350,000)	65 (23,000)
1,000	1,000 (35,000)	6.5 (2,300)*
100	100 (3,500)	0.65 (230)*
10	10 (350)	0.065 (23)*
1	1 (35)*	0.0065 (2.3)*

*It is very difficult to measure particulate counts below 10 per ft^3.

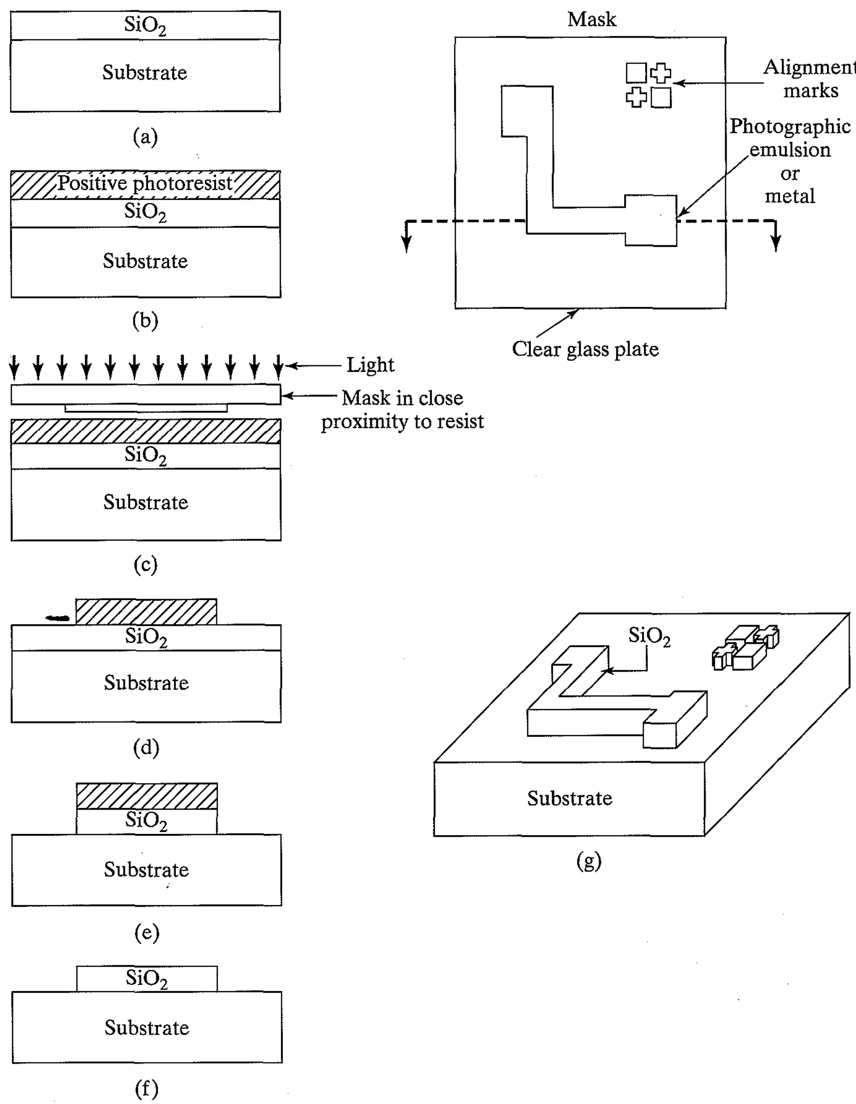

FIGURE 2.2

Drawings of a wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.

2.1.1 Wafer and Wafer Cleaning

IC fabrication starts with *n*- or *p*-type silicon wafers supplied with a specified resistivity. The wafers range in thickness from 250 to 500 μm. Two-hundred-mm (eight-inch)

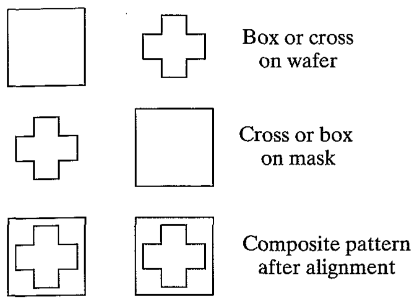

FIGURE 2.5

A simple set of alignment marks. At some steps a cross may be aligned within a box. At others, a box may be placed around the cross. The choice depends on the type of resist being used at a given mask step.

on the wafer. Manual operation of alignment and exposure equipment was used in early fabrication systems. However, VLSI/ULSI designs require extremely small geometrical features (minimum line width or space) and tight alignment tolerances. For example, 100 nm (0.1 μm) lithography will require a worst-case alignment error of 35 nm (mean + 3σ), and computer-controlled alignment systems are required to achieve these required levels of alignment precision.

With basic manual alignment equipment, the wafer is held on a vacuum chuck and carefully moved into position below the mask using an adjustable x–y stage. The mask is spaced 25 to 125 μm above the surface of the wafer during alignment. If contact printing is being used, the mask is brought into contact with the wafer after alignment.

Alignment marks are introduced on each mask and transferred to the wafer as part of the IC pattern. The marks are used to align each new mask level to one of the previous levels. A sample set of alignment marks is shown in Fig. 2.5. For certain mask levels, the cross on the mask is placed in a box on the wafer. For other mask levels, the box on the mask is placed over a cross on the wafer. The choice depends on the type of resist used during a given photolithographic step. Split-field optics are used to simultaneously align two well-separated areas of the wafer.

2.1.6 Photoresist Exposure and Development

Following alignment, the photoresist is exposed through the mask with high-intensity ultraviolet light. Resist is exposed wherever silicon dioxide is to be removed. The photoresist is developed with a process very similar to that used for developing ordinary photographic film, using a developer supplied by the photoresist manufacturer. Any resist that has been exposed to ultraviolet light is washed away, leaving bare silicon dioxide in the exposed areas of Fig. 2.6(d). A photoresist acting in the manner just described is called a *positive resist*, and the mask contains a copy of the pattern that will remain on the surface of the wafer. Windows are opened wherever the exposing light passes through the mask.

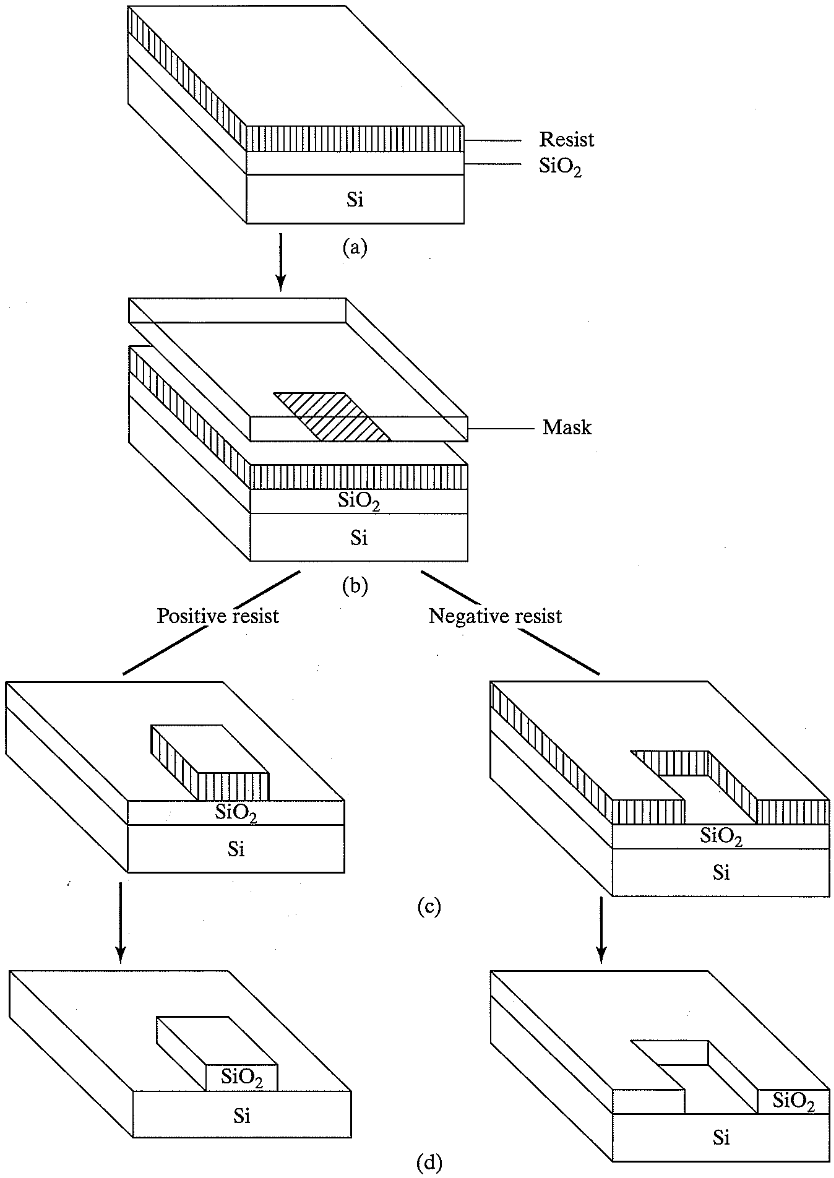

FIGURE 2.6

Resist and silicon dioxide patterns following photolithography with positive and negative resists.

Negative photoresists can also be used. A negative resist remains on the surface wherever it is exposed. Figure 2.6 shows simple examples of the patterns transferred to a silicon dioxide barrier layer using positive and negative photoresists with the same mask. Negative resists were widely used in early IC processing. However, positive resist yields better process control in small-geometry structures and is now the main type of resist used in VLSI processes.

EXHIBIT A-7

'S

Ninth New Collegiate Dictionary

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: OUT-OF-THE-WAY, SECLUDED ⟨a ~ cabin in the hills⟩ **4** : acting, acted on, or controlled indirectly or from a distance ⟨~ computer operation⟩; *also* : relating to the acquisition of information about a distant object (as by radar or photography) without coming into physical contact with it ⟨~ sensing instruments⟩ **5** : not arising from a primary or proximate action **6** : small in degree : SLIGHT ⟨a ~ possibility⟩ **7** : distant in manner : ALOOF — **re·mote·ly** *adv* — **re·mote·ness** *n*

re·mo·tion \ri-ˈmō-shən\ *n* (15c) **1** : the quality or state of being remote **2** : the act of removing : REMOVAL **3** *obs* : DEPARTURE

¹re·mount \(ˌ)rē-ˈmau̇nt\ *vb* [ME *remounten*, partly fr. *re-* + *mounten* to mount, partly fr. MF *remonter*, fr. *re-* + *monter* to mount] *vt* (15c) **1** : to mount (something) again ⟨~ a picture⟩ **2** : to furnish remounts to ~ *vi* **1** : to mount again **2** : REVERT

²re·mount \ˈrē-ˌmau̇nt, (ˌ)rē-ˈ\ *n* (1781) : a fresh horse to replace one no longer available

re·mov·al \ri-ˈmü-vəl\ *n* (1597) : the act or process of removing : the fact of being removed

¹re·move \ri-ˈmüv\ *vb* **re·moved**; **re·mov·ing** [ME *removen*, fr. OF *removoir*, fr. L *removēre*, fr. *re-* + *movēre* to move] *vt* (14c) **1 a** : to change the location, position, station, or residence of ⟨~ soldiers to the front⟩ **b** : to transfer (a legal proceeding) from one court to another **2** : to move by lifting, pushing aside, or taking away or off ⟨~s his hat in church⟩ **3** : to dismiss from office **4** : to get rid of : ELIMINATE ⟨~ a tumor surgically⟩ ~ *vi* **1** : to change location, station, or residence ⟨removing from the city to the suburbs⟩ **2** : to go away **3** : to be capable of being removed — **re·mov·abil·i·ty** \-ˌmü-və-ˈbil-ət-ē\ *n* — **re·mov·able** *also* **re·move·able** \ri-ˈmü-və-bəl\ *adj* — **re·mov·able·ness** \-ˈmü-və-bəl-nəs\ *n* — **re·mov·ably** \-blē\ *adv* — **re·mov·er** *n*

²remove *n* (1553) **1** : REMOVAL; *specif* : MOVE 2c **2 a** : a distance or interval separating one person or thing from another **b** : a degree or stage of separation

re·moved *adj* (1548) **1 a** : distant in degree of relationship **b** : of a younger or older generation ⟨a second cousin's child is a second cousin once ~⟩ **2** : separate or remote in space, time, or character

REM sleep *n* (1970) : a state of sleep that recurs cyclically several times during a normal period of sleep and that is characterized by increased neuronal activity of the forebrain and midbrain, by depressed muscle tone, and esp. in man by dreaming, rapid eye movements, and vascular congestion of the sex organs — called also *paradoxical sleep*, *rapid eye movement sleep*

re·mu·da \ri-ˈm(y)üd-ə\ *n* [AmerSp, relay of horses, fr. Sp, exchange, fr. *remudar* to exchange, fr. *re-* + *mudar* to change, fr. L *mutare* — more at MISS] (ca. 1892) : the herd of horses from which those to be used for the day are chosen

re·mu·ner·ate \ri-ˈmyü-nə-ˌrāt\ *vt* **-at·ed**; **-at·ing** [L *remuneratus*, pp. of *remunerare* to recompense, fr. *re-* + *munerare* to give, fr. *muner-*, *munus* gift — more at MEAN] (1523) **1** : to pay an equivalent for ⟨their services were generously *remunerated*⟩ **2** : to pay an equivalent to for a service, loss, or expense : RECOMPENSE *syn* see PAY — **re·mu·ner·a·tor** \-ˌrāt-ər\ *n* — **re·mu·ner·a·to·ry** \-rə-ˌtōr-ē, -ˌtȯr-\ *adj*

re·mu·ner·a·tion \ri-ˌmyü-nə-ˈrā-shən\ *n* (15c) **1** : something that remunerates : RECOMPENSE, PAY **2** : an act or fact of remunerating

re·mu·ner·a·tive \ri-ˈmyü-nə-rət-iv, -ˌrāt-\ *adj* (1627) **1** : serving to remunerate **2** : providing remuneration : PROFITABLE — **re·mu·ner·a·tive·ly** *adv* — **re·mu·ner·a·tive·ness** *n*

Re·mus \ˈrē-məs\ *n* [L] : a son of Mars slain by his twin brother Romulus

re·nais·sance \ˌren-ə-ˈsän(t)s, -ˈzän(t)s, -ˈsäⁿs, -ˈzäⁿs, *chiefly Brit* ri-ˈnās-ᵊn(t)s\ *n*, *often attrib* [F, fr. MF, rebirth, fr. *renaistre* to be born again, fr. L *renasci*, fr. *re-* + *nasci* to be born — more at NATION] (1845) **1** *cap* **a** : the transitional movement in Europe between medieval and modern times beginning in the 14th century in Italy, lasting into the 17th century, and marked by a humanistic revival of classical influence expressed in a flowering of the arts and literature and by the beginnings of modern science **b** : the period of the Renaissance **c** : the neoclassic style of architecture prevailing during the Renaissance **2** *often cap* : a movement or period of vigorous artistic and intellectual activity **3** : REBIRTH, REVIVAL

Renaissance man *n* (1906) : a person who has wide interests and is expert in several areas

re·nal \ˈrēn-ᵊl\ *adj* [F or LL; F *rénal*, fr. LL *renalis*, fr. L *renes* kidneys] (ca. 1656) : relating to, involving, or located in the region of the kidneys : NEPHRITIC

renal clearance *n* (1948) : CLEARANCE 3

re·na·scence \ri-ˈnas-ᵊn(t)s, -ˈnās-\ *n*, *often cap* (1864) : RENAISSANCE

re·na·scent \-ᵊnt\ *adj* [L *renascent-*, *renascens*, prp. of *renasci*] (ca. 1727) : rising again into being or vigor

re·na·ture \(ˌ)rē-ˈnā-chər\ *vt* **re·na·tured**; **re·na·tur·ing** \-ˈnāch-(ə-)riŋ\ [*re-* + *-nature* (as in *denature*)] (1926) : to restore (as a denatured protein) to an original or normal condition — **re·na·tur·ation** \(ˌ)rē-ˌnā-chə-ˈrā-shən\ *n*

ren·con·tre \räⁿ-kōⁿtrᵊ, ren-ˈkänt-ər\ *or* **ren·coun·ter** \ren-ˈkau̇nt-ər\ *n* [*rencounter* fr. MF *rencontre*, fr. *rencontrer*; *rencontre* fr. F] (1523) **1** : a hostile meeting or a contest between forces or individuals : COMBAT **2** : a casual meeting

ren·coun·ter \ren-ˈkau̇nt-ər\ *vt* [MF *rencontrer* to meet by chance or in hostility, fr. *re-* + *encontrer* to encounter] *archaic* (1549) : to meet casually

rend \ˈrend\ *vb* **rent** \ˈrent\; **rend·ing** [ME *renden*, fr. OE *rendan*; akin to OFris *renda* to tear, Skt *randhra* hole] *vt* (bef. 12c) **1** : to remove from place by violence : WREST **2** : to split or tear apart or in pieces by violence **3** : to tear (the hair or clothing) as a sign of anger, grief, or despair **4 a** : to lacerate mentally or emotionally **b** : to pierce with sound **c** : to divide (as a nation) into contesting factions ~ *vi* **1** : to perform an act of tearing or splitting **2** : to become torn or split *syn* see TEAR

¹ren·der \ˈren-dər\ *vb* **ren·dered**; **ren·der·ing** \-d(ə-)riŋ\ [ME *rendren*, fr. MF *rendre* to give back, yield, fr. (assumed) VL *rendere*, alter. of L *reddere*, partly fr. *re-* + *dare* to give & partly fr. *re-* + *-dere* to put — more at DATE, DO] *vt* (14c) **1 a** : to melt down : extract by melting ⟨~ lard⟩ **b** : to treat so as to convert into industrial fats and oils or fertilizer **2 a** : to transmit to another : DELIVER **b** : GIVE UP, YIELD **c** : to furnish for consideration, approval, or information: as **(1)** : to hand down (a legal judgment) **(2)** : to agree on and report (a verdict) **3 a** : to give in return or retribution **b (1)** : GIVE BACK, RESTORE **(2)** : REFLECT, ECHO **c** : to give in acknowledgment of dependence or obligation : PAY **d** : to do (a service) for another **4 (1)** : to cause to be or become : MAKE ⟨enough rainfall . . . to ~ irrigation unnecessary —P. E. James⟩ ⟨~ a person helpless⟩ **(2)** : IMPART **b (1)** : to reproduce or represent by artistic or verbal means : DEPICT **(2)** : to give a performance of **(3)** : to produce a copy or version of ⟨the documents are ~*ed* in the original French⟩ **(4)** : to execute the motions of ⟨~ a salute⟩ **c** : TRANSLATE **5** : to direct the execution of : ADMINISTER ⟨~ justice⟩ **6** : to apply a coat of plaster or cement directly to ~ *vi* : to give recompense — **ren·der·able** \-d(ə-)rə-bəl\ *adj* — **ren·der·er** \-dər-ər\ *n*

²render *n* (1647) : a return esp. in goods or services due from a feudal tenant to his lord

¹ren·dez·vous \ˈrän-di-ˌvü, -dā-\ *n*, *pl* **ren·dez·vous** \-ˌvüz\ [MF, fr. *rendez vous* present yourselves] (1591) **1 a** : a place appointed for assembling or meeting **b** : a place of popular resort : HAUNT **2** : a meeting at an appointed place and time **3** : the process of bringing two spacecraft together

²rendezvous *vb* **-voused** \-ˌvüd\; **-vous·ing** \-ˌvü-iŋ\; **-vouses** \-ˌvüz\ (1645) : to come together at a rendezvous ~ *vt* **1** : to bring together at a rendezvous **2** : to meet at a rendezvous

ren·di·tion \ren-ˈdish-ən\ *n* [obs. F, fr. MF, alter. of *reddition*, fr. LL *reddition-*, *redditio*, fr. L *redditus*, pp. of *reddere* to return] (1601) : the act or result of rendering: as **a** : SURRENDER **b** : TRANSLATION **c** : PERFORMANCE, INTERPRETATION

ren·dzi·na \ren-ˈjē-nə\ *n* [Pol *rędzina* rich limy soil] (1922) : any of a group of dark grayish brown intrazonal soils developed in grassy regions of high to moderate humidity from soft calcareous marl or chalk

¹ren·e·gade \ˈren-i-ˌgād\ *n* [Sp *renegado*, fr. ML *renegatus*, fr. pp. of *renegare* to deny, fr. L *re-* + *negare* to deny — more at NEGATE] (1583) **1** : a deserter from one faith, cause, or allegiance to another **2** : an individual who rejects lawful or conventional behavior

²renegade *vi* **-gad·ed**; **-gad·ing** (ca. 1611) : to become a renegade

³renegade *adj* (1705) **1** : having deserted a faith, cause, or religion for a hostile one **2** : having rejected tradition : UNCONVENTIONAL

re·nege \ri-ˈnig, -ˈneg, -ˈnēg, -ˈnāg\ *vb* **re·neged**; **re·neg·ing** [ML *renegare*] *vi* (1548) : DENY, RENOUNCE ~ *vi* **1** *obs* : to make a denial **2** : REVOKE **3** : to go back on a promise or commitment — **re·neg·er** *n*

re·ne·go·tia·ble \ˌrē-ni-ˈgō-sh(ē-)ə-bəl\ *adj* (1943) : subject to renegotiation ⟨~ mortgages⟩

re·ne·go·ti·ate \ˌrē-ni-ˈgō-shē-ˌāt\ *vt* (ca. 1934) : to negotiate again; *esp* : to readjust by negotiation to eliminate or recover excessive profits — **re·ne·go·ti·a·tion** \ˌrē-ni-ˌgō-s(h)ē-ˈā-shən\ *n*

re·new \ri-ˈn(y)ü\ *vt* (14c) **1** : to make like new : restore to freshness, vigor, or perfection ⟨as we ~ our strength in sleep⟩ **2** : to make new spiritually : REGENERATE **3 a** : to restore to existence : REVIVE **b** : to make extensive changes in : REBUILD **4** : to do again : REPEAT **5** : to begin again : RESUME **6** : REPLACE, REPLENISH ⟨~ water in a tank⟩ **7 a** : to grant or obtain an extension of or on **b** : to grant or obtain an extension on the loan of ⟨~ a library book⟩ ~ *vi* **1** : to become new or as new **2** : to begin again : RESUME **3** : to make a renewal (as of a lease) — **re·new·er** *n*

syn RENEW, RESTORE, REFRESH, RENOVATE, REJUVENATE mean to make like new. RENEW implies so extensive a remaking that what had become faded or disintegrated now seems like new ⟨efforts to *renew* a failing marriage⟩ RESTORE implies a return to an original state after depletion or loss ⟨*restored* a fine piece of furniture⟩ REFRESH implies the supplying of something necessary to restore lost strength, animation, or power ⟨lunch *refreshed* my energy⟩ RENOVATE suggests a renewing by cleansing, repairing, or rebuilding ⟨the apartment has been entirely *renovated*⟩ REJUVENATE suggests the restoration of youthful vigor, powers, and appearance ⟨the change in jobs *rejuvenated* her spirits⟩

re·new·able \-ˈn(y)ü-ə-bəl\ *adj* (1727) **1** : capable of being renewed ⟨~ contracts⟩ **2** : capable of being replaced by natural ecological cycles or sound management practices — **re·new·abil·i·ty** \-ˌn(y)ü-ə-ˈbil-ət-ē\ *n* — **re·new·ably** \-ˈn(y)ü-ə-blē\ *adv*

re·new·al \ri-ˈn(y)ü-əl\ *n* (1681) **1** : the act or process of renewing : REPETITION **2** : the quality or state of being renewed **3** : something renewed (as a subscription to a magazine) **4** : something used for renewing; *specif* : an expenditure that betters existing fixed assets **5** : the rebuilding of a large area (as of a city) by a public authority

reni- *or* **reno-** *comb form* [L *renes* kidneys] : kidney ⟨*reniform*⟩

re·ni·form \ˈrē-nə-ˌfȯrm, ˈren-ə-\ *adj* [NL *reniformis*, fr. *reni-* + *-formis* -form] (ca. 1753) : suggesting a kidney in outline

re·nin \ˈrē-nən, ˈren-ən\ *n* [ISV, fr. L *renes*] (1906) : a proteolytic enzyme of the kidney that plays a major role in the release of angiotensin

re·ni·ten·cy \ˈren-ə-tən-sē, ri-ˈnit-ᵊn-\ *n* (1613) : RESISTANCE, OPPOSITION

re·ni·tent \ˈren-ə-tənt, ri-ˈnit-ᵊnt\ *adj* [F or L; F *rénitent*, fr. L *renitent-*, *renitens*, prp. of *reniti* to struggle against, fr. *re-* + *niti* to strive — more at NISUS] (1701) **1** : resisting physical pressure **2** : resisting constraint or compulsion : RECALCITRANT

ren·min·bi \ˈren-ˈmin-ˈbē\ *n pl* [Chin (Pek) *ren²min²* (fr. *ren²* human + *min²* people) people's + *bi⁴* currency] (ca. 1957) : the currency of the People's Republic of China consisting of yuan

ren·net \ˈren-ət\ *n* [ME, fr. (assumed) ME *rennen* to cause to coagulate, fr. OE *gerennan*, fr. *ge-* together + (assumed) OE *rennan* to cause to run; akin to OHG *rennen* to cause to run, OE *rinnan* to run — more at RUN] (15c) **1 a** : the contents of the stomach of an unweaned animal and esp. a calf **b** : the lining membrane of a stomach or one of its compartments (as the fourth of a ruminant) used for curdling milk; *also* : a preparation of the stomach of animals used for this purpose **2 a** : RENNIN **b** : a substitute for rennin

ren·nin \ˈren-ən\ *n* (1897) : an enzyme that coagulates milk and is used in making cheese and junkets; *esp* : one from the mucous membrane of the stomach of a calf

\ə\ abut \ᵊ\ kitten, F table \ər\ further \a\ ash \ā\ ace \ä\ cot, cart \au̇\ out \ch\ chin \e\ bet \ē\ easy \g\ go \i\ hit \ī\ ice \j\ job \ŋ\ sing \ō\ go \ȯ\ law \ȯi\ boy \th\ thin \t͟h\ the \ü\ loot \u̇\ foot \y\ yet \zh\ vision \à, k, ⁿ, œ, ᵫ, ue, ue, ᵞ\ see Guide to Pronunciation

EXHIBIT A-8

Webster's Third New International Dictionary

OF THE ENGLISH LANGUAGE

UNABRIDGED

A Merriam-Webster
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Webster's third new international dictionary of
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Philip Babcock, 1902–1972. II. Merriam-Webster Inc.
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ISBN 0-87779-201-1 (blue Sturdite)
ISBN 0-87779-206-2 (imperial buckram)

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41KP88

Excerpt, Page 1921

[1]**re·move** \rə'müv, rē'-\ *vb* [ME *removen, remeven*, fr. OF *remouvoir, removoir*, fr. L *removēre*, fr. *re-* + *movēre* to move — more at MOVE] *vt* **1 :** to change or shift the location, position, station, or residence of (as in order to reestablish) **:** SHIFT, TRANSFER — usu. used with *to* and specified place ⟨~ the troops to the front⟩ ⟨~ the family to the seashore⟩; *specif* **:** to transfer (a pending case) for original hearing or trial from one court to another in the same or another jurisdiction — compare REMOVAL OF CAUSES **2 :** to move by lifting, pushing aside, or taking away or off **:** put aside, apart, or elsewhere ⟨~*s* his hat in the house⟩ ⟨~ a book from a shelf to examine it⟩ **3 :** to force (one) to leave a place or to go away: as **a :** to dismiss from office **b :** ASSASSINATE **c :** to take away by death **4 :** to get rid of as though by moving **:** ERADICATE, ELIMINATE ⟨~ the causes of poverty⟩ ~ *vi* **1 :** to change location, station, or residence ⟨~ from their town house to the country⟩ **2 :** to go away **:** DISAPPEAR, DEPART **3 :** to be capable of being removed ⟨a bottle cap that ~*s* easily⟩ **syn** see MOVE

[2]**remove** \"\ *n* -s **1 a :** REMOVAL; *specif* **:** the transfer of one's business or of one's domestic belongings from one location or dwelling house to another **:** MOVE **b** *archaic* **:** the act of removing a horse's shoe to dress the hoof **c** *Brit* **:** a change of dishes during a meal **d** *Brit* **:** promotion of a pupil to the next form **2 a :** a distance (as a space, time, or divergence of state) separating one person or thing from another **:** distance apart or away ⟨at a short ~ upon the same platform was an officer —Ambrose Bierce⟩ ⟨her poems . . . work best at a slight ~ from the personal —Richard Wilbur⟩ **b** (1) **:** a degree distant (as in derivation or relationship) **:** a grade or stage of separation from the immediate or direct **:** a step apart or away ⟨such a popular song . . . simply repeats, at many ~*s*, a motif of the conventional behavior of the courtly lover —R.A.Hall b.1911⟩ ⟨a primary and intense experience . . . which men at best know only at second ~ —M.F.A. Montagu⟩ — compare FIRSTHAND (2) **:** a degree of lineal consanguinity **:** a generation removed ⟨only at one ~ from the villager —G.M.Trevelyan⟩ ⟨the sixteen sire lines . . . of these famous racehorses at the fourth ~ —Dennis Craig⟩ **3** *obs* **:** ABSENCE **4 :** an intermediate form between two others in an English school

EXHIBIT A-9

THIN FILM PROCESSES

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planes to etch at different rates. Various orientations of single-crystal substrates may thus etch very differently in a given etchant, and substrates of varying roughness may also exhibit large differences in etch rates.

Several additional specific factors affecting etching reactions in various types of materials will be noted in the discussions of insulators and semiconductors (Sections III.A and III.B, respectively).

C. Etching Techniques and Processes

The choice of the etching technique to be used for a given situation depends upon the material to be etched, the requirements of pattern generation, the necessary etching reagents, the etching processes involved, and other factors such as economic considerations.

1. Immersion Etching

The simplest technique is liquid chemical immersion or dip etching where the masked or unmasked object is submerged in the etch solution. Mechanical agitation is usually desirable as it improves the uniformity and control of the etching process by enhancing the exchange and mixing of spent etching solution at the solid surface with fresh solution. This also avoids local overheating in the case of exothermic reactions, thereby maintaining a uniform and controllable etching rate. Bubbles of gas (usually H_2) that may form as a reaction product can cling to the solid surface and inhibit uniform etching. The addition of a surface-active agent to the etch solution can prevent bubble accumulation. A sufficiently large ratio of etchant to material being etched should be employed to minimize reactant depletion and to maintain the reaction temperature and the rate of attack.

2. Spray Etching

Spray etching is useful for generating patterns in relatively thick films or substrates, especially if steep pattern walls are desired, since the impinging etch solution imparts a variable degree of directionality to the process. The etching rate is increased over that of immersion etching, and can be regulated by the amount of pressure applied and the size of the droplets. Good process control and uniformity can be attained because fresh etchant is rapidly and constantly supplied to the reaction site, while the reaction products are continuously removed. Spray etching lends itself to automation, and commercial etching machines are available for many specific applications.

3. Electrolytic Etching

Electrically conductive or semiconductive materials are frequently etched by application of external emf potentials. Electropolishing of metals and semiconductors is a good example of this technique. The rate and selectivity of etching can be controlled by the potential and/or the current density applied. Electrolytic etching is considerably more complicated than other techniques, but can yield results not otherwise attainable. Specific conditions will be described for various materials in the text and in the etching tables.

4. Gas-Phase Etching

High-temperature etching in the gas or vapor phase is generally used for chemically inert materials that cannot be etched readily in liquid reagents. A different application is for *in situ* etching of semiconductor substrates immediately prior to epitaxial film growth in the same reactor to avoid surface contamination that would result by other techniques.

5. Mechanical–Chemical Polishing

This technique is used in semiconductor wafer preparation when a relatively defect-free surface is required. The combination of slow liquid chemical surface etching with gentle mechanical abrasion to continuously remove products from the etching reaction can result in a high-quality surface polish if carefully optimized conditions are observed, as will be described in Section III.B.

6. Isotropic versus Anisotropic Processes

Isotropic or nonpreferential etching proceeds at an equal rate in all directions. Amorphous materials of uniform composition etch isotropically, whereas many crystalline materials etch both isotropically and anisotropically. Anisotropic or preferential etching depends on the crystallographic orientation of the material and on the etching reagent used. If polishing action is desired, isotropic etching conditions must be selected to achieve a structureless surface. If structural shaping is the objective, as in the formation of deep depressions having side walls of a specific taper angle, anisotropic conditions are required. Both liquid and gas-phase etching can be used for these two types of etching processes.

7. Selective Etching Processes

Selectivity refers to the differences in etch rate between different materials, or between compositional or structural variations of the same ma-

terial. It is one of the most important factors in applied etching. Most technological etching processes must be controllably selective because the material to be etched is usually part of a structure that consists of several material components. Selectivity in etching is achieved by proper choice of etching technique and etchant composition within the constraints of the systems.

Various degrees of etching selectivity are desirable for particular purposes. For example, pattern etching of Si_3N_4 or Al_2O_3 films in hot H_3PO_4 using an etch-resistant deposited SiO_2 film as the etch mask illustrates a high degree of etching selectivity. On the other hand, controlled partial etching selectivity of dielectric layer composites is important in taper etching, where a desired edge contour can be attained on the basis of etch rate differences of the component layers. In this case, a faster etching dielectric "taper-control" layer is formed over the dielectric to be beveled [46]. Numerous other important applications of selective etching have been described [26, 27, 48, 49].

8. *Fusion Techniques and Other Processes*

Certain highly etch-resistant materials can be etched by treatment with molten salts (often caustics or borax) at high temperature. Several examples will be noted in Sections IV.B and IV.D.

Surface oxidation by thermal or anodic treatments, followed by chemical stripping of the oxide films formed, can also be considered an etching process. However, only the second step, the etching of the oxides, will be discussed here (Section III.A).

D. Pattern Delineation Etching for Thin Films

In many instances, etching processes are used to produce certain patterns in thin films. Selected portions of the film are masked by another thin film coating material which is unaffected by the etchant to be used for patterning. Etching is then carried out so as to remove all the film material in the unprotected regions. The protective coating film is then usually stripped, leaving the desired pattern in the underlying thin film.

Pattern etching is obviously a much more complex process than simple overall surface etching. In addition to selecting the etchant, choosing a masking material is of prime importance; good adhesion of this coating to the substrate, coating integrity, adequate resolution, and resistance to the etchant are the main considerations. Ease in patterning the mask coating is important; otherwise this procedure becomes an etching process itself, requiring yet another mask.

EXHIBIT A-10

United States Patent [19] [11] **4,404,731**

Poleshuk [45] **Sep. 20, 1983**

[54] **METHOD OF FORMING A THIN FILM TRANSISTOR**

[75] Inventor: **Michael Poleshuk**, Webster, N.Y.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **307,463**

[22] Filed: **Oct. 1, 1981**

[51] **Int. Cl.**^{3} **H01L 21/363**

[52] **U.S. Cl.** **29/571**; 29/578; 29/591

[58] **Field of Search** 29/571, 578, 591; 430/314, 319

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"Effect of Thermal Annealing on Thin Film Transistors Processed by Photoengraving", Shepherd et al., J. Vac. Sci. Technol., vol. 17, No. 1,-Jan./Feb. 1980, pp. 485-488.

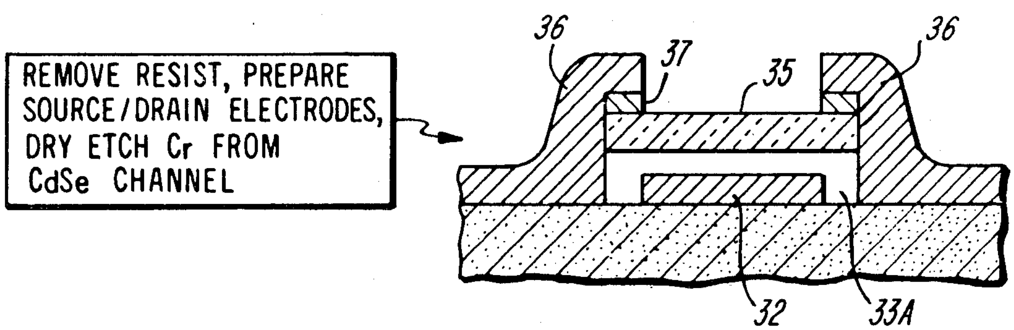
Primary Examiner—G. Ozaki

Attorney, Agent, or Firm—Robert A. Chittum; John B. Mason

[57] **ABSTRACT**

In the formation of a thin film device, integrity of the semiconductor-insulator and semiconductor-conductor interfaces is preserved by depositing layers of insulator, semiconductor, and conductor in successive sequence under continuous vacuum. In a preferred embodiment, the method minimizes contamination exposure of the critical interfaces between semiconductor and gate insulator and semiconductor and source-drain contacts of a thin film transistor.

14 Claims, 14 Drawing Figures



APPLY RESIST LAYER

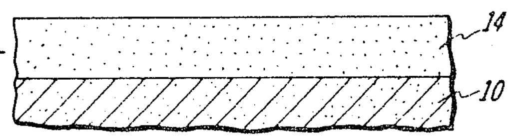


FIG. 1A

EXPOSE AND DEVELOP RESIST LAYER TO FORM GATE MASK

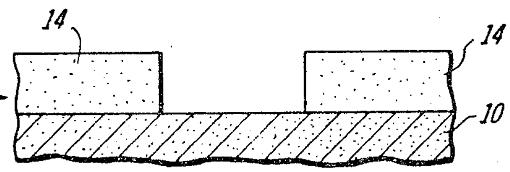


FIG. 1B

DEPOSIT GATE CONDUCTOR (Al) LAYER

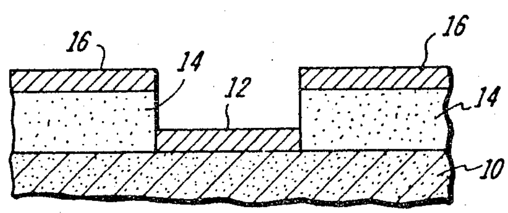


FIG. 1C

REMOVE RESIST TO DELINEATE GATE

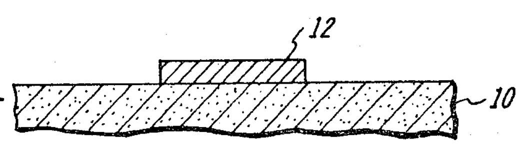


FIG. 1D

DEPOSIT INSULATOR (SiO_2) LAYER

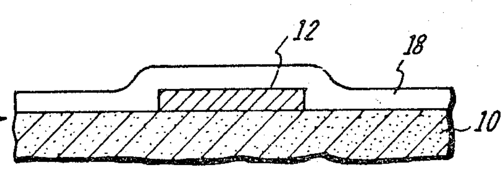


FIG. 1E

APPLY RESIST LAYER

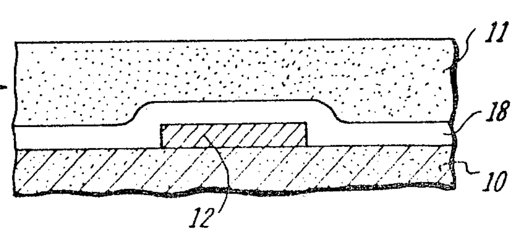


FIG. 1F

EXPOSE AND DEVELOP RESIST TO FORM ADDITIVE MASK

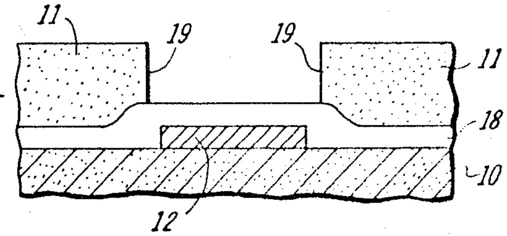


FIG. 1G

IN SINGLE PUMPDOWN DEPOSIT INSULATOR (SiO_2)~13 SEMICONDUCTOR (CdSe), ~15 AND SOURCE/DRAIN (Cr)~17 CONTACT LAYERS

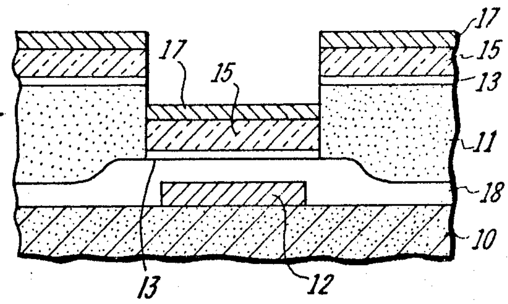


FIG. 1H

REMOVE RESIST, LIFTING OFF OVERLYING LAYERS

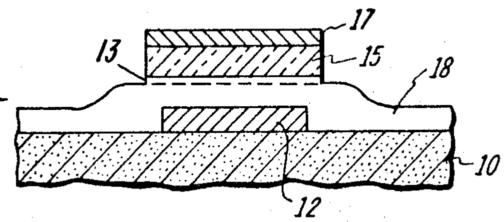


FIG. 1I

PREPARE SOURCE/DRAIN ELECTRODES BY ADDITIVE PROCESS

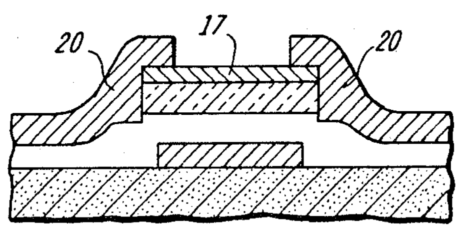


FIG. 1J

DRY ETCH Cr FROM CdSe CHANNEL USING SOURCE/DRAIN ELECTRODES AS MASK

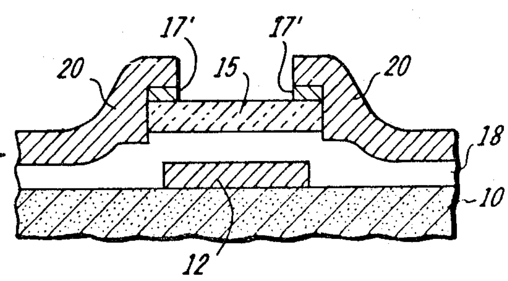


FIG. 1K

DELINEATE GATE ELECTRODE

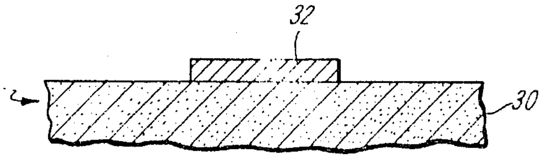


FIG. 2A

IN SINGLE PUMPDOWN DEPOSIT INSULATOR (SiO_2) SEMICONDUCTOR (CdSe) & SOURCE/DRAIN (Cr) CONTACT LAYERS THROUGH ADDITIVE MASK

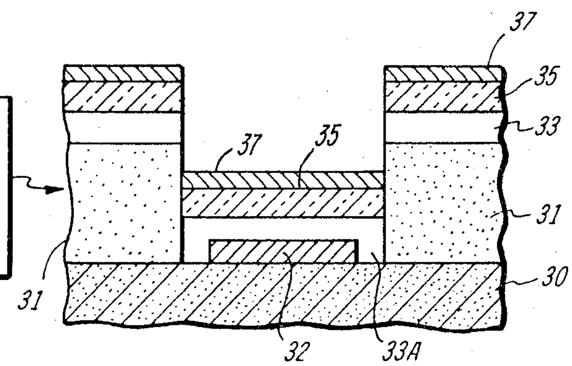


FIG. 2B

REMOVE RESIST, PREPARE SOURCE/DRAIN ELECTRODES, DRY ETCH Cr FROM CdSe CHANNEL

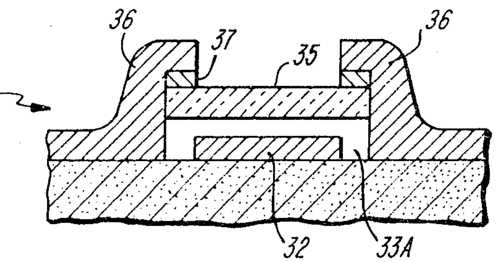


FIG. 2C

METHOD OF FORMING A THIN FILM TRANSISTOR

BACKGROUND OF THE INVENTION

This invention broadly relates to a process for forming a device by selective deposition and patterning of thin film layers of insulative, semiconductive, and conductive materials. More particularly, the invention concerns an improved method of forming such a device wherein thin film layers of insulator, semiconductor, and metal are deposited in successive sequence under continuous vacuum. The invention has particular utility in the photolithographic fabrication of thin film transistors and arrays thereof. In the fabrication of such devices, single pump down formation of the semiconductor-gate insulator and semiconductor-source/drain contact interfaces minimizes the exposure of these critical interfaces to contamination during wet processing.

With increasing demand for high device density, photolithographic processes have become increasingly popular as economical means for fabricating thin film transistors. Such techniques are particularly advantageous in the preparation of high density thin film transistor drivers for high resolution, large area displays, such as those incorporating liquid crystal or electroluminescent media.

Conventional photolithographic techniques characteristically employ wet chemistry processes to selectively define patterned layers of conductive and insulative materials. These wet processes include chemical polish etching for initial substrate preparation, structural, or pattern delineation, etching to create a relief structure geometry, and photoresist processing.

The electrical performance and the stability of surface field effect transistors are critically dependent upon the quality of the semiconductor-insulator interface and upon the ohmic properties of source drain contacts to semiconductor interface. The quality of both interfaces can be impaired by impurity contamination arising from exposure from each material (i.e., conductor, insulator, and semiconductor) surface to wet processing. Such contamination increases the densities of interface states and reduces conduction modulation. Incorporation of ionic species present in the chemical solution alters the otherwise predictable threshold voltages. Charge transfer processes at interface states and field aided migration of mobile ionic species induces operational instabilities into the devices. Impurity related contact barriers degrade transconductance by limiting current and crowding transistor characteristics. These wet processing induced degradations create device characteristics problems such as non-reproducability from batch to batch and non-uniformity among devices within a single batch. These problems are particularly pernicious when a large area transistor array is being fabricated for use in a display. In this context, the demands of high quality image resolution necessitates a high degree of uniformity among transistor characteristics and an extremely high yield of operable devices.

The present invention provides a process for overcoming the disadvantages which can arise from exposure of critical surfaces of the constituent layers of the thin film device to wet processing.

SUMMARY OF THE INVENTION

The present invention provides methods for preserving the integrity of the interfaces between layers of

semiconductor and insulator and semiconductor and conductor during formation of a thin film device. This is achieved by depositing the layers of insulator, semiconductor, and conductor in the desired sequence under continuous vacuum, i.e., in a single vacuum pump down operation. This technique effectively seals, or encapsulates, the damage (i.e., contamination or impurity) sensitive semiconductor so that subsequent wet processing steps do not adversely affect the electrical characteristics of the device by contaminating critical interfaces. As well, sequential deposition of these layers under vacuum affords protection of the semiconductor interfaces against degradation by air borne contaminants.

In accordance with one particularly advantageous embodiment, the invention minimizes contamination exposure of the critical interfaces between the semiconductor and gate and semiconductor and source and drain contacts of a thin film transistor. Exemplary of this method is a fabrication sequence utilizing aluminum, silicon dioxide, cadmium selenide, and chromium and aluminum, for the gate electrode, gate insulator, semiconductor, and source and drain contacts, respectively. The initial step in this sequence is the formation of the aluminum gate electrode on a portion of a surface of a substrate by, for example, additive photolithographic delineation. As typical and well known in the prior art, for example, U.S. Pat. No. 4,040,073 to Luo or U.S. Pat. No. 4,132,586 to Schaible et al, the gate electrode extends to the edge of the substrate for a single transistor or to an integrally and concurrently formed bus bar that extends to the edge of the substrate for an array of transistors. Contact tabs may be formed or attached to the gate electrode or bus bar at the substrate edge. An additive photoresist mask is then formed for definition of the semiconductor pad. The silicon dioxide gate insulator, cadmium selenide, and chromium contact layers are then sequentially deposited through the apertures in the additive mask during a single vacuum pump down to form the critical semiconductor-insulator interface and semiconductor-source and drain contacts. During subsequent lift off removal of the photoresist mask, the chromium contact layer functions as a protective cap over the semiconductor pad, preventing harmful interaction between the semiconductor and the stripping solution, i.e., the solvent per se or ionic species contained therein. Two steps remain for completion of the thin film transistor, removal of that portion of the chromium layer overlying the conducting channel of the semiconductor and definition of the aluminum source and drain network. The aluminum source and drain electrodes are formed by additive processing to provide a structure wherein respective source and drain electrodes are separated by a gap corresponding to the width of the conducting channel of the semiconductor layer and exposing portions of the chromium layer. In the final process step, the aluminum source drain network structure functions as a substractive mask through which chromium is selectively removed from the thin film transistor conducting channel by dry etching techniques.

The dry etching techniques, e.g., plasma etching, are preferred for this final step because of the high degree of etch selectivity and "cleaniness" which are characteristic of such processes.

Alternatively, the sequence for fabricating a thin film transistor includes the step of depositing an initial layer

of insulative material to cover the gate electrode and the entire surface of the substrate on which the gate electrode is formed. Utilization of this process to provide a "full" rather than patterned insulator layer over the substrate and gate electrode is particularly advantageous as a means for enhancing the insulation between source and gate electrode gate crossovers in a multitransistor array.

In a preferred variation of the foregoing processes, the side wall surfaces of the openings in the photoresist mask used to find the semiconductor pad are coated with a thin film of insulator, e.g. silicon dioxide, prior to the single pump down sequential deposition of the critical device layers. This step insures minimum contamination of the electrically active regions of the device by complete isolation thereof from organic materials present during removal of the photoresist mask.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–1K are diagramatic cross-sectional views of a structure being fabricated in accordance with a preferred embodiment of the invention, as well as a flow chart describing steps within the process.

FIGS. 2A–2C are diagramatic cross-sectional views of a device at selected stages of an alternative fabrication sequence.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1A–1D illustrate the formation of a gate electrode **12** upon a surface of substrate **10**. A broad range of materials may be employed for substrate **10**, subject to the general limitation that the material chosen be insulative relative to the material selected for gate electrode **12**. The exact choice of a material for substrate **10** will, of course, depend upon the particular application in which the thin film transistor is utilized. When employed as a driver of an element in a liquid crystal display, for example, substrate **10** would comprise one of the planar glass plates which are typically employed to contain the liquid crystal media. In other applications, utility may dictate that substrate **10** be composed of other insulative material, such as ceramics, semiconductors, plastic materials, and the like. Quite satisfactory results have been obtained with the use of a barium aluminum borosilicate composition sold commercially by Corning Glass Works of Corning, N.Y. under the trademark Corning 7059 Glass.

The additive, or lift off, technique illustrated in FIGS. 1A–1D is well known. As shown, this method begins with the application of a covering layer of resist material **14** on the upper surface of substrate **10**. Resist **14** can comprise conventional photo or electron beam materials which are characterized by radiation-induced alteration in solubility that enables subsequent removal with aqueous solutions. A suitable material is Shipley's AZ 1350B or AZ 1350J sold by Shipley Company, Inc., of Newton, MA. Resist **14** is applied in any conventional manner, as for example, by spin coating. Thereafter, in accordance with well known photolithographic techniques, resist layer **14** is processed into an additive mask by conventional steps of exposure, development, and removal of selective pattern areas thereof.

In the next step, as illustrated in FIG. 1C, a 1,000 Angstrom layer of aluminum is deposited, as by vacuum evaporation, sputtering, or the like, over the surface of the mask substrate. This aluminum layer is deposited through the apertures in the photoresist mask onto the surface of the substrate **10** to form gate electrode **12** and on top of the remaining portions of resist layer **14** as indicated at **16**.

Next, to arrive at the gate structure shown in FIG. 1D, the remaining portions of resist **14** and the overlying aluminum layer **16** are removed using conventional lift off removal techniques, i.e., by exposing the structure to a solvent suited to the solubility of the resist **14**.

It will be appreciated that the gate structure shown in FIG. 1D could be produced by subtractive processing, rather than through the additive steps illustrated in FIGS. 1A–1D.

After formation of the gate, as shown in FIG. 1E, a blanket layer of aluminum oxide **18** or silicon dioxide is deposited over the gate electrode **12** and the exposed surface of substrate **10**. This insulative layer can be applied in any conventional manner, as for example, by evaporation or sputtering within a suitable vacuum device. As noted above, coverage of the complete active surface of the substrate is desirable for multi transistor arrays. From a practical standpoint, complete coverage of the entire surface of the substrate is not preferred, since the contact fingers for the array bus lines are typically located around the periphery of the substrate. However, as will be discussed hereinafter with reference to FIGS. 2A–2C, it is not essential that the complete substrate be covered with an insulator. Where such a layer is employed, a thickness range of about 2,0000 Å to about 4,000 Å is preferred.

A second blanket layer of resist **11** is applied over insulator **18** as illustrated in FIG. 1F. As with resist **14**, various solvent soluble materials may be chosen for the resist layer **11**, the same being applied by any of the well known techniques such as spinning, spraying, dipping or the like. Again utilizing standard lithographic techniques, resist layer **11** is exposed and developed in a pattern corresponding to the desired dimensions of the semiconductor pad for the thin film transistor as illustrated by the structure of FIG. 1G.

The patterned resist layer **11** is used as an additive mask for depositing, in successive sequence, layers of insulator (SiO_2) **13**, semiconductor (CdSe) **15**, and conductor (Cr) **17**. It is of critical importance to the invention that these layers be deposited under the continuous vacuum of a single pump down operation. This is accomplished by placing the structure of FIG. 1G into any suitable vacuum chamber and reducing the pressure to about 5×10^{-7} torr. Thereafter, utilizing conventional deposition techniques of the integrated circuit fabrication art, the layers of SiO_2, CdSe, and Cr are deposited in succession. The ambient for deposition of SiO_2 could consist of 5×10^{-5} partial pressure of oxygen. Referring to FIG. 1H, it will be appreciated that the initial deposition of a thin additional layer of insulator **13** onto the pre-existing insulator layer **18** provides a clean insulative interface for the subsequently deposited semiconductor layer **15**, isolating the same from any contaminants or impurities introduced onto the surface of insulator **18** during the process of forming the additive mask thereon or during handling of the substrate or exposure thereof to air. A thickness of about 800 Å for insulator layer **13** has been found to be adequate for these purposes. Following deposition of the layer of SiO_2, a layer of CdSe is deposited to a thickness of about 300 Å followed by deposition of a layer of Cr to a thickness of about 500 Å.

Utilizing conventional lift off removal techniques, the layer of resist **11** and all of the layers overlying it are

removed by exposing the coated substrate of FIG. 1H to a suitable solvent for resist **11**. Such solvents include acetone and other commercially available strippers.

In a preferred alternative embodiment of the invention, maximum immunity against contamination of the electronically active device regions is achieved by lining the side walls **19** of the apertures in resist layer **11** with a thin film of insulator (SiO_2) prior to deposition of layers **15** and **17**. This additional step (which is not shown) completely isolates the critical regions of the device from the organic materials utilized in the subsequent processing. Such a protective layer of silicon dioxide can be deposited as a separate step or concurrently with the deposition of layer **13**.

After removal of the lift off mask, the structure is as shown in FIG. **11**. During lift off removal of the resist and overlying layers, the chromium film acts as a protective cap to isolate the upper surface of semiconductor pad **15** from processing contaminants in the solvent. Referring briefly to FIG. **1K**, the completed thin film transistor structure is shown having source and drain electrodes **20** electrically connected to the semiconductor through chromium contacts **17'**. To arrive at the structure, source and drain electrodes **20** are formed by conventional additive processing to yield the structure of FIG. **1J**. In the context of the illustrative example, the source and drain electrodes **20** are aluminum and are patterned so as to expose the chromium contact layer **17**.

In the final step, the source and drain electrode network is employed as a subtractive mask during selective dry etching of chromium from the conducting channel of the thin film transistor. Dry etching techniques are preferred for this step because of the characteristic cleanliness of such methods as well as the high degree of directionality offered thereby. Plasma etching utilizing a reaction gas, e.g. CCl_4 vapor in the air or oxygen has been found to be particularly effective in removing chromium in the embodiment illustrated herein. The conductive material chosen for the source and drain contacts **20** must be resistant to the plasma employed to etch the conductive contact layer **17**. While other materials may be used, aluminum deposited to a desired thickness of about 1,000 Angstroms has been demonstrated to be sufficiently resistant to plasma etching in a reaction gas, such as mentioned above. It will be appreciated that selection of other materials for the source and drain electrodes **20** and the contacts **17'** and the choice of a suitable ambient for the selected materials other than that described herein are possible.

An alternative sequence for fabricating a thin film transistor is illustrated in FIGS. **2A–2C**. FIG. **2A** illustrates a gate electrode **32** formed upon a substrate **30**. This structure corresponds to the structure illustrated in FIG. **1D** and is produced by any suitable deposition techniques, such as the additive process discussed in conjunction with FIGS. **1A–1D**.

After delineation of the gate electrode **32**, an additive mask is formed by exposure and development of a resist layer **31** which is applied to the structure of FIG. **2A**. Unlike the process discussed with reference to FIGS. **1A–1K**, there is no initial deposition of an insulator layer such as layer **18** of FIG. **1E**. Instead, the resist is coated directly over the exposed surfaces of substrate **30** and gate electrode **32**. Thereafter, using standard lithographic techniques, portions of the resist layer are selectively removed to expose the gate electrode **32** and portions of the surface of substrate **30** adjacent the gate electrode to form an additive mask. In the next step, layers of insulator **33**, **33A** (SiO_2) semiconductor **35** (CdSe), and conductor **37** (Cr) are deposited onto the mask structure during a single vacuum pump down operation by means such as discussed in conjunction with FIG. **1H**. The resulting structure is illustrated in FIG. **2B**, wherein it will be noted that, by virtue of the selected pattern in the resist mask, that portion of the deposited insulator designated **33A** forms a gate insulator layer which covers both upper and side surfaces of gate electrode **32**.

With process steps identical to those described with respect to FIGS. **1I** through **1K**, the lift off mask is removed, source and drain electrodes **36** are delineated, and the chromium contact layer plasma etched using the source drain network as a dry etch. These steps produce the thin film transistor shown in FIG. **2C**.

An array of transistors of the type shown in FIG. **2c** is completed by depositing crossover insulators (not shown) for dielectric isolation of source/drain bus lines from gate line **32** by methods well known in the art.

I claim:

1. An improved method of forming a thin film transistor on a substrate of the type having a gate electrode of a conductive material formed on a portion of a surface of the substrate and extending to the edge of the substrate to provide means for contact therewith, wherein the improved method comprises the steps of:

(a) forming a first insulator layer covering the gate electrode and the remaining portion of the surface of the substrate on which said electrode is formed, the end of the gate electrode at the substrate edge not being covered to permit contact therewith;

(b) forming on said first insulator layer, a masking layer having a predetermined opening therein exposing a portion of said first insulator layer;

(c) sequentially depositing, under vacuum, a second insulator layer, a semiconductor layer, and a conductive contact layer on said masking layer and on the exposed portion of said first insulator layer;

(d) removing said masking layer and the portions of the second insulator layer, the semiconductor layer, and the conductive contact layer deposited thereon;

(e) selectively forming a third conductor layer to define source and drain contacts to said semiconductor layer, said third conductor layer having a predetermined opening therein exposing a portion of said conductive contact layer; and

(f) removing the exposed portion of said conductive contact layer to expose said semiconductor layer.

2. The method of claim **1**, wherein said step (f) comprises removing the exposed portions of said conductive contact layer by dry etching.

3. The method of claim **2** wherein said dry etching comprises plasma etching.

4. The method of claim **2** wherein said dry etching comprises ion beam milling.

5. A method of forming an active region of a thin film transistor on a substrate having a gate electrode deposited thereon which extends to the edge of the substrate to provide means for contact therewith, the method comprising depositing thin film layers of an insulator, a semiconductor, and a conductive metal upon a portion of the gate electrode and a surface portion of the substrate adjacent the gate electrode portion in successive sequence under continuous vacuum, said surface portion of the substrate and gate electrode portion being

exposed by a predetermined opening in a mask to define and delineate the exact transistor dimensions by said opening.

6. The method of claim 5, wherein said mask comprises a photoresist mask formed by removing a portion of a photoresist masking layer deposited upon said substrate to expose the surface portion of said substrate, gate electrode portion, and side wall surfaces of the opening in said photoresist mask.

7. The method of claim 6, further including:

(a) removing said photoresist mask and the portions of the insulator, semiconductor, and conductive metal deposited thereon;

(b) selectively forming a second conductor layer to define separate source and drain contacts to said semiconductor, said source and drain contacts having a space therebetween to expose a portion of the conductive metal; and

(c) removing the exposed portion of the conductive metal to expose the semiconductor so that separate remaining portions of the conductive metal lie between the semiconductor and portions of the source and drain contacts.

8. The method of claim 6, further including the step of depositing a thin film of insulating material on the side wall surfaces of the opening in said photoresist mask prior to the step of depositing said layers of insulator, semiconductor, and metal.

9. The method of claim 6, wherein a thin film of insulating material is deposited on the side wall surfaces of the opening in said photoresist mask concurrently with the deposition of said layer of insulator.

10. A method of forming a thin film transistor on a substrate having a gate electrode of a conductive metal on a portion of a surface of the substrate, the gate electrode having an extension leading to one edge of the substrate to provide means for contact therewith after a transistor is formed thereover, the method comprising the steps of:

(a) forming a masking layer covering the surface of said substrate having the gate electrode, said masking layer having a predetermined opening therein exposing said gate electrode and a portion of the surface of said substrate adjacent said electrode;

(b) sequentially depositing, under vacuum, an insulator layer, a semiconductor layer, and a conductive contact layer on said masking layer and on the gate electrode and exposed portion of the surface of said substrate;

(c) removing said masking layer and the portions of the insulator layer, semiconductor layer, and the conductive contact layer deposited thereon;

(d) selectively forming a third conductor layer to define source and drain contacts to said semiconductor layer, said third conductor layer having a predetermined opening therein exposing a portion of said conductive contact layer; and

(e) removing the exposed portion of said conductive contact layer to expose said semiconductor layer.

11. The method of claim 10, wherein said step (e) comprises removing the exposed portions of said conductive contact layer by dry etching.

12. The method of claim 11 wherein said dry etching comprises plasma etching.

13. The method of claim 11 wherein said dry etching comprises ion beam milling.

14. A method of forming an array of thin film transistors on a substrate having a predetermined pattern of gate electrodes of conductive material formed on a surface of the substrate, the gate electrodes having extensions which connect to at least one bus bar of conductive material formed on the substrate surface which extends to the edge of the substrate whereat means for contact is provided for the bus bar, the method comprising the steps of:

(a) forming a first insulator layer covering the gate electrodes, gate electrode extensions, bus bar and selected remaining portions of the surface of the substrate on which said electrodes, extensions and bus bar are formed;

(b) forming on said first insulator layer a masking layer having predetermined pattern of openings therein exposing portions of said first insulator layer;

(c) sequentially depositing, under vacuum, a second insulator layer, a semiconductor layer, and a conductive contact layer on said masking layer and on the exposed portions of said first insulator layer;

(d) removing said masking layer and the portions of the second insulator layer, the semiconductor layer, and the conductive contact layer deposited thereon;

(e) selectively forming a third conductor layer to define source and drain contacts to said semiconductor layer, said third conductor layer having a predetermined pattern of openings therein exposing portions of said conductive contact layer; and

(f) removing the exposed portions of said conductive contact layer to expose said semiconductor layer by dry etching.

* * * * *

EXHIBIT B-2

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

LG. PHILIPS LCD CO. LTD,	:	
Plaintiff,	:	
v.	:	Civil Action No. 05-292-JJF
TATUNG COMPANY, TATUNG COMPANY OF AMERICA, INC., CHUNGWHA PICTURE TUBES LTD., and VIEWSONIC CORP.,	:	
Defendants.	:	

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Attorneys for Defendants.

MEMORANDUM OPINION

June 13, 2006
Wilmington, Delaware

Joseph J. Farnan Jr.

Farnan, District Judge:

Plaintiff L.G. Philips LCD Co., LTD ("LPL") filed this patent infringement action against Defendants Tatung Company, Tatung Company of America, Inc., Chungwha Picture Tubes, LTD., and ViewSonic Corporation (collectively "CPT"). LPL alleges that CPT has infringed U.S. Patent No. 5,019,002 ("the '002 patent"). LPL's Complaint (D.I. 1) also alleges infringement of U.S. Patent No. 6,738,121 ("the '121 patent"), but LPL has withdrawn all claims relating to that patent. (D.I. 180.) Presently before the Court is the claim construction dispute of the parties. The parties briefed their respective positions, and the Court held a Markman hearing on March 20, 2006. This Memorandum Opinion provides the Court's construction of the claim terms and phrases disputed by the parties.

BACKGROUND

The Patent at issue in this lawsuit relates to flat panel, display screens and methods of manufacturing them that include electrostatic discharge guard rings to protect the active elements of the display from electrostatic discharge during and after manufacturing. In their briefing and at the Markman hearing, the parties disputed twenty-six terms and phrases from the claims of both the '002 patent and the '121 patent. By its Order dated March 22, 2006 (D.I. 155), the Court ordered the parties to select a reduced number of terms and phrases to be

construed by the Court. The Court allowed LPL to submit a maximum of five terms or phrases and CPT a maximum of eight. (D.I. 155.) Following the parties' submissions of the terms and phrases to be construed, LPL filed a Notice Of Voluntary Withdrawal Of Claims Relating To U.S. Patent No. 6,738,121 (D.I. 180). As a result of that withdrawal and the fact that one claim term was submitted by both parties, there are currently six claim terms and phrases in dispute: "interconnecting," "outer electrostatic discharge guard ring," "resistance," "corner pad," "removing said outer guard ring and row and column interconnections," and "pickup pad."

DISCUSSION

I. Legal Principles Of Claim Construction

Claim construction is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 977-78 (Fed. Cir. 1995), aff'd, 517 U.S. 370, 388-90 (1996). In interpreting a claim, a court should look first to the intrinsic evidence, i.e. the patent itself, including the claims and the rest of the specification, and, if in evidence, the prosecution history. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). Although it is within the sound discretion of a court to use extrinsic evidence as an aid in construing a claim, extrinsic evidence is "unlikely to result in a reliable interpretation of patent claim scope unless considered in the

context of the intrinsic evidence." Phillips v. AWH Corp., 415 F.3d 1303, 1319 (Fed. Cir. 2005) (en banc).

A claim term should be construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Markman, 52 F.3d at 986. However, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1313. Thus, the specification is usually "dispositive; it is the single best guide to the meaning of a disputed term." Id. at 1315 (quoting Vitronics, 90 F.3d at 1582). In other words, a claim term can be given its correct construction only within the context of "what the inventors actually invented and intended to envelop with the claim." Phillips, 415 F.3d at 1316.

II. Construction Of The Disputed Terms and Phrases

The language of independent claim 1 and dependent claims 3 and 7 is representative of the disputed terms and phrases. In full, claim 1 provides (emphasis added):

> 1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:
> providing a substrate;
> forming a pattern of pixels on said substrate;
> forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;
> forming an outer electrostatic discharge guard

> ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and
>
> removing said outer guard ring and row and column interconnections prior to completion of the display.

('002 patent, col. 8, l. 65 - col. 9, l. 12.) In full, claim 3 provides (emphasis added): "3. The method as defined in claim 1 including forming at least one pickup pad coupled to said resistance via a shunt switching element." (Id. col. 9, ll. 16-18.) In full, claim 7 provides (emphasis added): "7. The method as defined in claim 1 including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections." (Id. col. 9, ll. 29-33.)

A. Construction of "Interconnecting"

LPL contends that the term "interconnecting" should be construed as "shorting." (D.I. 135 at 12.) LPL argues that "'interconnecting' was used throughout the entire intrinsic record in a manner consistent with this single meaning." (Id.) CPT contends that "shorting" is impermissibly vague because the specification uses that term in a variety of contexts. (D.I. 144 at 6.) CPT proposes instead the construction "electrically connecting with conductors." (D.I. 164 at 1.)

The Court agrees with CPT that LPL's proposed construction

is vague. Substituting "shorting" for "interconnecting" would not clarify the meaning of "interconnecting," but rather would make it more ambiguous. In the '002 patent's specification, "short" is used in at least four different ways: the path taken by an unintended, destructive discharge of a static potential ('002 patent, col. 2, ll. 57-62); a physical defect in electrical components resulting in an unintended current pathway (Id., col. 4, ll. 27-28); a deliberate re-routing of an electrostatic discharge via a shunt transistor (Id., col. 7, ll. 35-41); and a deliberate connection between electrical elements to provide an alternate current pathway (Id., col. 5, ll. 65-68). Only the last of these is consistent with LPL's proposed construction of "interconnecting".

LPL contends that CPT's proposed construction of "electrically connecting with conductors" improperly limits the term "interconnecting" to a single embodiment by specifying that the electrical connection must be made with conductors. (D.I. 158 at 2.) However, the consistent use of a claim term by the inventor in the specification may serve to limit the scope of a claim. Nystrom v. Trex Co., Inc., 424 F.3d 1136, 1145 (Fed. Cir. 2005). Here, CPT's proposed construction is consistent with the inventor's use of "interconnecting" throughout the '002 patent's

specification.[1] "Interconnecting" is consistently described or illustrated in figures as using "lines", "shorts", or "jumpers", i.e. conductors, to connect electrical elements. (See e.g., '002 patent, col. 5, ll. 65-68; col. 6, ll. 6-9; col. 6, ll. 42-43; col. 8, ll. 5-7.) Therefore, the Court will construe "interconnecting" to mean "electrically connecting with conductors."

B. Construction of "Removing Said Outer Guard Ring and Row and Column interconnections"

LPL contends that the phrase "removing said outer guard ring and row and column interconnections" does not require construction, but that the proper construction, if one is necessary, is "physically disconnecting said guard ring and row and column interconnections." (D.I. 135 at 23-24.) CPT's proposed construction is "electrically disconnecting the interconnections between rows and between columns, and electrically disconnecting rows and columns from the outer guard ring." (D.I. 137 at 12.) The Court agrees with LPL's construction.

The parties' dispute hinges on the meaning of "removing," with LPL contending that it means "physically disconnecting" and

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[1] Defendants' proposed construction is also consistent with the use of "interconnecting" in U.S. Patent 4,820,222 ("the '222 patent), which has the same inventor as the '002 patent and is incorporated by reference in the '002 patent. ('002 patent, col. 2, ll. 30-36.)

Defendants contending that it means "electrically disconnecting." CPT's construction depends on its assertion that "removing" means "removing a part or component from an electronic circuit." (D.I. 144 at 3; D.I. 138 at 9.) However, as it is used throughout the specification, "removing" is more logically interpreted as referring to the removal of the guard ring and row and column interconnections from the display panel. (See '002 patent, Abstract ("the external guard ring is removed prior to completion of the display"); col. 2, ll. 64-65 ("the external guard ring is removed at the end of the display manufacturing process"); col. 8, ll. 27-30 ("[t]he outer ESD guard ring . . . is removed prior to completion of the display").) Thus, the intrinsic evidence indicates that "removing" is used to mean physical disconnection and separation such that the outer guard ring and row and column interconnections are not included in the finished display panel. Therefore, the Court will construe "removing said outer guard ring and row and column interconnections" as "physically disconnecting said guard ring and row and column interconnections."

C. Construction of "Outer Electrostatic Discharge Guard Ring"

LPL's proposed construction of the phrase "outer electrostatic discharge guard ring" is "a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges." (D.I. 158 at

2.) CPT's proposed construction is "a ring of conductor, located external to the inner electrostatic discharge guard ring if the two rings are used together, for draining off electrostatic buildup to prevent electrostatic discharge." CPT does not dispute that the outer guard ring is "a closed or open ring, or open L or C-shaped line." (D.I. 144 at 6.) The parties do dispute whether the guard ring functions to prevent electrostatic discharge ("ESD") or only to protect against damage caused by ESD.[2] The parties also dispute the meaning of "outer."

The specification consistently refers to the function of the ESD guard rings as protecting the active elements of the display from ESD rather than preventing ESD altogether. (See '002 patent, Abstract ("At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines."); col. 2, ll. 61-61 ("An external guard ring can be formed, which provides protection during manufacture of the displays . . ."); col. 8, ll. 27-29 ("The outer ESD guard ring provides ESD protection only during manufacture of the display . . .").) CPT points out that the specification uses the word "prevent" or "preventive" to describe the function of the ESD rings. (D.I. 164 at 4.) However, in

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[2] CPT refers to this dispute as "insignificant," but, nevertheless, maintains the position that the proper construction refers to prevention of ESD rather than protection from ESD. (D.I. 164 at 4.)

both of the locations cited, the specification is referring to the prevention of damage caused by ESD rather than to the prevention of ESD itself.

The central dispute over the phrase "outer electrostatic discharge guard ring" is whether "outer" is used in reference to an inner ESD ring or to the entire display panel. CPT contends that "outer" must refer to the outer guard ring's position relative to the inner guard ring. (D.I. 137 at 8.) This contention is untenable. Independent claims 1 and 19 include an outer ESD guard ring, but no inner ESD guard ring. In the context of those claims, CPT's proposed construction would render the adjective "outer" meaningless.

On the other hand, LPL contends that "outer" refers to the outer guard ring's position relative to the active matrix display. CPT concedes that "active matrix display" as used in the '002 patent and in LPL's proposed construction means the entire finished display panel. (D.I. 164 at 3.) CPT argues that the Court should reject LPL's proposed construction because it is based on "the erroneous notion that the outer ring must be physically removed at the end of the manufacture." (Id.) As the Court concluded in section II.B. above, however, the intrinsic evidence indicates that physical removal of the outer guard ring is precisely what the patent teaches. Therefore, the Court will construe "outer electrostatic discharge guard ring" as "a closed

or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."

D. Construction of "Resistance"

The parties agree that one of ordinary skill in the art would understand "resistance" to mean a physical property of a material or device characterized by opposition to the flow of electric current. (D.I. 135 at 13; D.I. 137 at 9.) They also agree that in the '002 patent, "resistance" is used to denote a circuit component. (D.I 135 at 13; D.I. 160 at 2.) LPL contends that because "[a]ll circuit components . . . have the characteristic of resistance," the Court should construe "resistance" as "any component used to cause a voltage drop during current flow." (D.I. 135 at 13.) CPT's proposed construction is "[a] resistance, as it is used in the claims, means a resistor, which is a circuit element that has a specified resistance to the flow of electrical current. A resistance does not include switching elements such as transistors and diodes." (D.I. 137 at 9.)

LPL's proposed construction cannot be correct because, as CPT points out, (D.I. 137 at 12), it would exclude the single preferred embodiment that incorporates a "resistance." (See '002 patent, col. 8, ll. 1-48.) The only purposes stated for the "resistance" in that embodiment are to provide an "ESD short for

high electrostatic potentials . . . ," (Id., col. 8, l. 31), and to minimize "the discharge current surge . . .," (Id., col. 8, l. 35). Thus, "resistance" as used in that embodiment, would not fall within the scope of LPL's proposed construction of "any component used to cause a voltage drop during current flow." A claim construction that excludes a preferred embodiment "is rarely, if ever, correct and would require highly persuasive evidentiary support. . . ." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed. Cir. 1996) (citations omitted). The Court finds no such evidentiary support in this case.

On the other hand, CPT's proposed construction unnecessarily limits "resistance" to one specific electric component, a resistor. There is no support in the intrinsic record for such a narrow interpretation. Moreover, a person skilled in the art would certainly understand the meaning of "resistor" so it is logical to conclude that the inventor would have chosen that term had he intended to refer only to that specific component.

LPL correctly notes, (D.I. 163 at 3), that it is improper to import limitations from a preferred embodiment into the claims. See JVW Enterprises, Inc. v. Interact Accessories, Inc., 424 F.3d 1324, 1335 (Fed. Cir. 2005). However, "there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." Phillips v. AWH Corp., 415 F.3d 1303, 1323 (Fed.

Cir. 2005) (quoting Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186-87 (Fed. Cir. 1998)). Here, because "resistance" is used in the claims in a manner somewhat different from its ordinary meaning to one of skill in the art, the only guidance as to how the Court should construe the term is how it is used in the single embodiment in which it appears. That embodiment mentions a "resistance" three times:

> The [ESD guard ring] line **210** is connected to the other set of gate or source lines by a shunt line **224**, a shunt transistor **226** and a large resistance **228**, such as 100 K ohms (illustrated schematically). . . . The resistance provides an ESD short for high electrostatic potentials which can be incurred during manufacturing . . . . The resistance minimizes the discharge current surge . . . .

('002 patent, col. 8, ll. 23-34.) In the claims, the term "resistance" is used consistently to denote only a circuit component used to couple the outer ESD guard ring to the interconnected row and column lines and the pickup pad. (See e.g. Id., col. 9, ll. 63-65; col. 10, ll. 6-8.)

Reading the claims in light of the specification, which describes the "resistance" only in general terms, the Court concludes that the patentee intended the claims and this embodiment in the specification to be coextensive at least in regard to the term "resistance".[3] Therefore, the Court will

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[3] The Court also notes that the patentee explicitly stated that certain elements of the invention could vary from the specific descriptions in that embodiment, but did not include the "resistance" among those elements. ('002 patent, col. 8, ll. 49-

construe "resistance" as "a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge."

E. Construction of "Corner Pad"

LPL contends that the term "corner pad" does not require construction, but that the proper construction, if one is necessary is "a reference mark for cutting" (D.I. 135 at 24.) CPT contends that the Court should construe "corner pad" as "a pad of metal or other conductive materials that is located at the corner of an outer guard ring, and electrically connected with the outer ring" (D.I. 137 at 15.) CPT argues, (Id.), and LPL does not dispute, that "corner pad" has no inherent meaning to one of ordinary skill in the art and thus can be understood only within the context of the '002 patent's claims and specification. LPL does concede that "[o]ne of ordinary skill in the art would understand the term 'pad' to be a conductive area." (D.I. 135 at 15; D.I. 143 at 15.)

The term "corner pad" appears in only one embodiment in the specification. (See '002 patent, col. 8, ll. 1-48.) That embodiment describes three features of a "corner pad." First, it is connected to each other corner pad by conductive lines of the outer guard ring. (Id., col. 8, ll. 8-11.) Second, it can be grounded. (Id., col. 8, ll. 11-12.) Third, it provides

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62.)

alignment for the scribe lines. (Id., col. 8, ll. 12-15.) The second feature is explicitly optional, so it need not be included in the Court's construction. The third feature is specifically claimed, so it too need not be included in the Court's construction. (See, e.g., Id., col. 9, ll. 29-33 ("7. The method as defined in claim **1** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.")) Therefore, the Court concludes that LPL's proposed construction of "a reference mark for cutting" is unnecessary and would be redundant. The location of the corner pad is also specifically claimed as being "on at least one corner of the display." (See, e.g., Id., col. 9, l. 30.) Thus CPT's inclusion of "located at the corner of an outer guard ring" in its proposed construction is both unnecessary and inaccurate.

The remaining issue is whether the "corner pad" must be electrically connected to the outer guard ring. CPT bases its contention that the "corner pad" must be "electrically connected with the outer ring" on a single sentence from the specification: "A corner pad **208** is connected to each other corner pad (not illustrated) by respective outer conductive lines **210** and **212** of the guard ring **200**." (Id., col. 8, ll. 8-11.) The Court concludes that it would be improper to import this limitation from the specification into the claims. Therefore, to the extent

that "corner pad" requires construction, the Court will construe it as "an area of conductive material."

F. <u>Construction of "Pickup Pad"</u>

LPL's proposed construction of "pickup pad" is "a conductive area used to electrically connect the back plane to the front plane" (D.I. 135 at 14.) CPT's proposed construction is "a pad located at the corner region of a backplane for aligning the frontplane and backplane" (D.I. 137 at 13.) CPT contends, and LPL does not dispute, that the term "pickup pad" has no inherent meaning to one of ordinary skill in the art, and thus, can be understood only within the context of the intrinsic evidence. (D.I. 137 at 13.) The parties agree, however, that "pad" would be understood by one of ordinary skill in the art to mean a conductive area. (D.I. 135 at 15; D.I. 143 at 15; D.I. 160 at 3.) The Court concludes that neither proposed construction is appropriate and will decline to construe "pickup pad."

LPL's contention that the "pickup pad" is used to electrically connect the back plane to the front plane has no support in the intrinsic evidence. Neither the specification nor the claims of the '002 patent mentions any electrical connection between the front plane and the back plane via the "pickup pad". Both teach only the electrical connection of the "pickup pad" with other elements on the back plane. Thus, LPL's proposed construction cannot be correct.

CPT's proposed construction would violate the doctrine of claim differentiation. In this context, claim differentiation "refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim." Curtiss-Wright Control Corp. v. Velan, Inc., 438 F.3d 1374, 1380 (Fed. Cir. 2006) (citing Nazomi Communications, Inc. v. Arm Holdings, PLC., 403 F.3d 1364, 1370 (Fed. Cir. 2005)). In the '002 patent, claim 5 depends from claim 3.[4] Claim 3 claims "[t]he method as defined in claim **2** including forming at least one pickup pad coupled to said resistance via a shunt switching element." ('002 patent, col. 9, ll. 16-18.) Claim 5 claims "[t]he method as defined in claim **3** including forming a corner on the said pad to align the front plane and back plane of the display." (Id., col. 9, ll. 23-25.) To construe "pickup pad" as CPT proposes, as "a pad . . . for aligning the frontplane and backplane," would be to read the limitation from claim 5 into claim 3, rendering claim 5 superfluous and violating the doctrine of claim differentiation.

All of the significant attributes of the "pickup pad" mentioned in the specification are also specifically claimed. (Compare, '002 patent, col. 8, ll. 18-39, with id. col. 9, ll. 16-28.) Therefore, the Court concludes that no further

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[4] The discussion that follows applies identically to claims 16 and 14, 23 and 21, and 34 and 32.

construction of the term "pickup pad" is necessary.

CONCLUSION

An Order consistent with this Memorandum Opinion will be entered setting forth the meaning of the disputed terms and phrases in the '002 patent.

EXHIBIT B-3

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG.PHILIPS LCD CO., LTD., Plaintiff/Counterclaim Defendant, v. TATUNG COMPANY; TATUNG COMPANY OF AMERICA, INC.; CHUNGHWA PICTURE TUBES, LTD.; AND VIEWSONIC CORPORATION, Defendants/Counterclaim Plaintiffs.	Civil Action No. 05-292 (JJF)

PLAINTIFF'S MEMORANDUM IN SUPPORT OF
ITS PROPOSED CLAIM CONSTRUCTIONS

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March 8, 2006

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MEMORANDUM IN SUPPORT OF
PLAINTIFF'S PROPOSED CLAIM CONSTRUCTIONS

Plaintiff LG.Philips LCD Co., Ltd. ("LPL") submits this brief in support of its constructions of disputed claim terms of LPL's U.S. Patent No. 5,019,002 ("the '002 Patent," Ex. A) and U.S. Patent No. 6,738,121 ("the '121 Patent," Ex. B) at issue in this litigation.

I. NATURE AND STAGE OF THE PROCEEDING

On May 13, 2005, LPL filed its Complaint for Patent Infringement against Defendants Tatung Co. ("Tatung"), Tatung Company of America, Inc. ("Tatung America"), Chunghwa Picture Tubes, Ltd. ("CPT"), and ViewSonic Corporation ("ViewSonic") (collectively, the "Defendants") alleging infringement of both the '002 Patent and the '121 Patent (collectively, the "Patents-in-Suit"). On September 2, 2005, Defendants filed their Answers and Counterclaims, alleging invalidity and non-infringement of the Patents-in-Suit. The matter is set for trial beginning on July 17, 2006.

LPL and Defendant CPT (a subsidiary of Tatung) are in the business of manufacturing and selling liquid crystal displays ("LCDs"), which are used in popular flat-screen products such as televisions and computer monitors. Defendants Tatung, Tatung America, and ViewSonic manufacture and/or sell products containing LCDs, including LCDs manufactured by CPT. Briefly, the '002 Patent relates to methods for preventing damage to LCDs due to electrostatic discharge, which occurs during the manufacture of LCDs. The '121 Patent also relates to LCDs with tape carrier packages, which are structures for mounting integrated circuits on LCDs.

During the exchange of claim terms and meet and confer process prior to this brief, LPL set forth nine (9) terms for construction, while Defendants initially set forth thirty-eight (38) terms for construction, but subsequently withdrew eleven (11) of those terms. The parties discussed their proffered terms and definitions, leading Defendants to withdraw one (1)

additional term. Defendants' approach has necessitated the parties' briefing of the remaining disputed twenty-six (26) terms.

The disputed claim terms in the Patents-in-Suit should be construed in accordance with either: (1) their ordinary meanings, as a "heavy presumption" exists that claims terms be given their ordinary and customary meaning; or (2) definitions compelled by a review of the intrinsic evidence, where applicable. Further, it is LPL's position that nearly all of the terms set forth below do not require any further construction, because their meanings are clear to one of ordinary skill in the art. Nevertheless, because Defendants have requested their legal construction, LPL briefs them herein.

II. STATEMENT OF THE FACTS

A. The Technology at Issue

A brief overview of the LCD structure, in general, and the manufacturing method of thin-film-transistor liquid crystal displays ("TFT-LCDs"), in particular, is necessary to provide the proper context for the claim constructions discussed below.

The use of flat screens for computer monitors and televisions is relatively new. Traditionally, computer monitors have used cathode ray tubes ("CRT") to create images for viewing. A CRT uses a tube that is large and heavy compared to a flat screen, which is thin and light. As a result, the use of flat screens for computer monitors and other products has become very popular with consumers.

TFT-LCDs are a type of flat panel display used to generate images in many popular flat screen products. A typical LCD panel includes upper and lower polarizers, upper and lower glass substrates (*i.e.*, a front plane and a back plane) equipped with circuit elements, and liquid crystal between the glass substrates. Images on a screen are then created by electronically controlling the amount of light allowed through the LCD panels. The typical light source is

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either a backlight unit or reflected ambient light. How much light is allowed through the LCD panels depends on the orientation of the crystal molecules in the liquid crystal as controlled by electrical signals.

The electrical signals control the orientation of the crystal molecules in the liquid crystal by creating an electric field between the upper and lower glass substrates. To create the electric field, a voltage is applied to what are known as pixel electrodes. As each pixel electrode corresponds to a pixel or dot on the screen, it is possible to control the emission of light through the LCD panels for each pixel or dot on the screen by controlling the electrical signals sent to the various pixel electrodes.

The pixel electrodes are part of the circuit elements that are in LCD panels. Circuit elements are generally manufactured by depositing layers of conductive material and then patterning such layers by a photolithography process. The circuit elements create a matrix of rows and columns of circuit control lines, with a pixel contact connected to a pixel electrode, and a control element between the control line rows and columns. During manufacture, these rows and columns can also provide a conductive pathway for damaging electrostatic discharge, otherwise known as "ESD."

The matrix arrangement allows controlling the electrical signals to the various pixel electrodes. Each row and column is equipped with a contact pad through which electrical signals are sent. Generally, one driving circuit is used for each row or column control line. In this way, an electrical signal can be fed to an entire row containing a large number of pixels. Then another electrical signal can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties.

So-called active-matrix displays employ thin film transistors (TFTs), or tiny switching transistors and capacitors arranged in the matrix on a glass substrate. A TFT is generally associated with each particular pixel. This arrangement is beneficial because the capacitor is able to hold the charge until the next refresh cycle. Accordingly, by carefully controlling the amount of voltage supplied to a pixel, the orientation of the liquid crystal molecules can be manipulated just enough to allow some light through. By doing this in very exact, very small increments, LCDs can create a gray scale. Most displays today offer at least 256 levels of brightness per pixel.

The electrical signals are fed to the rows and columns by driving integrated circuits (D-ICs). In order to create the desired images on the screen, it is necessary to have D-ICs that can feed the appropriate signals to the various rows and columns of the active matrix display, thereby activating the correct pixels in accordance to the signals from the printed circuit board (PCB). These D-ICs are generally located between the PCB and the LCD panels.

This case concerns LPL's significant innovations relating to: (1) improving how D-ICs are mounted on the liquid crystal panel of an LCD (the '121 Patent); and (2) methods for providing protection against electrostatic discharge during the manufacture of active matrix displays (the '002 Patent).

B. <u>The Patents-in-Suit</u>

1. <u>The '002 Patent</u>

The '002 Patent, entitled "Method of Manufacturing Flat Panel Backplanes Including Electrostatic Discharge Prevention and Displays Made Thereby," was filed on July 12, 1988, and names Scott H. Holmberg as the inventor. The '002 Patent issued on May 28, 1991.

The '002 Patent relates to methods to protect the circuit elements from damage caused by electrostatic discharge that is accidentally fed into the active matrix. During the manufacture of

the device, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of row and column lines. Electrostatic discharge is undesirable because it generally causes a short, and thus a burn out of the pixel, thereby rendering the pixels defective, resulting in black dots on the screen. When this occurs, the LCD panel manufacturer may be unable to use the entire back plane of the active matrix display. The high occurrence of unusable product in turn causes the manufacturer to suffer a radically increased manufacturing cost.

To protect the device from electrostatic discharge during manufacture, the '002 Patent discloses a process that employs electrostatic discharge guard rings around the active elements of the display. To protect the matrix from electrostatic discharge, the manufacturing process of the '002 Patent employs an outer electrostatic discharge guard ring, which is connected to the rows and columns. The rows and columns are also connected together with jumpers. Furthermore, because the outer electrostatic discharge guard ring is not necessary after manufacturing, the outer electrostatic discharge guard ring is positioned outside of the active matrix display. In this manner, after manufacture is completed, the outer electrostatic discharge guard ring can be easily removed. The '002 Patent also discloses an inner electrostatic discharge guard ring located inside the outer electrostatic discharge guard ring to also serve to protect against electrostatic discharge.

Upon examination of the application, the Examiner rejected claims 1-6, 8-17, 19-24, and 26-35 under 35 U.S.C. § 103 as being obvious over the combined teachings of U.S. Patent Nos. 4,803,536, 4,455,739, 4,586,242, and 4,736,271. The remaining claims were indicated as containing allowable subject matter. Ex. F, Office Action, mailed March 31, 1989, at p. 3.

In response to the Office Action, no amendments were made to the claims to overcome the prior art rejection. Instead, Applicants distinguished claims 1 and 19 over the cited prior art

stating that the prior art did not teach removable resistive stripes as required by these claims. Furthermore, with respect to claims 10 and 28, Applicants argued that the cited prior art also did not teach or suggest inner guard rings as claimed. Ex. G, Proposed Response, filed July 2, 1990, at p 2. In light of these remarks, the claims were allowed. Ex. H, Notice of Allowance, mailed December 7, 1990.

2. The '121 Patent

The '121 Patent, entitled "Tape Carrier Package with Dummy Bending Part and Liquid Crystal Display Employing the Same," was filed on March 23, 2001, and names Sai Chang Yun and Eun Yeong An as the inventors. The '121 Patent issued on May 18, 2004 and claims foreign priority to a Korean Patent Application filed on March 31, 2000.

Generally, a tape carrier package (TCP) is used as the mounting method for the D-ICs. The PCB is folded to the rear side of an LCD panel by bending the TCP, mounted with a driving integrated circuit and connected between the back plane (lower glass substrate) and the PCB. To allow for the TCP to bend, a portion of its base film is removed. The TCP is equipped with leads that connect the D-ICs to the PCB, to receive the signals from the PCB, and to the contact pads of the rows and columns in the active matrix, to deliver the output signals.

During the manufacture of LCD panels, it is important to be able to form and connect all components without damage. One problem that often arises during the connection of the D-ICs is warping of the glass substrate caused by the high heat and pressure in the manufacturing process. Specifically, the thermal expansion forces and the thermal contraction forces generated at the time of thermal-pressing the TCP to the liquid crystal panel result in warping of the back plane. Such warping of the glass substrate is undesirable because it causes a brightness variation on the screen.

Using LPL's patented technology, the tape carrier package is mounted on the liquid crystal panel in such a way that does not cause a brightness variation in the LCD. The TCP of the '121 patent has at least one bending part, which is a bendable part of the TCP where base film has been removed to enable the tape carrier package to bend. The TCP of the '121 Patent also has at least one dummy bending part, which is a part of the TCP where base film has been removed, and has a function other than bending. The dummy bending part functions, *inter alia*, to distribute stress caused by thermal expansion applied to the liquid crystal panel when the tape carrier package is bonded to the liquid crystal panel with high heat and pressure. In doing so, it is possible to prevent stress-induced deformation of the back plane of the liquid crystal panel, thereby preventing the occurrence of brightness differences on the LCD screen.

After a first examination of the patent application that ultimately matured into the '121 Patent, claims 1, 4-7, 9-12, and 14 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,398,128. Ex. C, Office Action, mailed March 24, 2003, at p. 2. Applicants distinguished over this prior art on the basis that it did not teach or suggest "wherein the dummy bending part is formed at a position, close to any one of the output pad part or the input pad part, where the tape carrier package is not folded," and amended all rejected claims to include this limitation. Ex. D, Amendment, filed July 22, 2003, at p. 11. The rejected claims were subsequently allowed. Ex. E, Notice of Allowance, mailed November 21, 2003.

III. SUMMARY OF THE ARGUMENT

A. Terms or Phrases of the '002 Patent That Should be Construed

1. The terms "interconnecting;" "resistance;" and "shunt switching element" should be construed in accordance with their ordinary meanings.

2. The terms "pick up pad;" "outer electrostatic discharge guard ring;" and "inner electrostatic discharge guard ring" should be construed in accordance with definitions compelled by a review of the intrinsic evidence.

B. <u>Terms or Phrases of the '002 Patent That Should Not be Construed</u>

The following terms or phrases of the '002 Patent, proposed by Defendants, should not be construed because their meanings are clear to one of ordinary skill in the art: "interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;" "electrostatic discharges;" "coupled to said interconnected row and column lines via a resistance;" "removing said outer guard ring and row and column interconnections;" "corner pad;" "scribe line;" and "aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections."

C. <u>Terms or Phrases of the '121 Patent That Should be Construed</u>

1. The term "bending part" and the phrase "pad part extending from the integrated circuit chip" should be construed in accordance with their ordinary meanings.

2. The term "dummy bending part" and the phrases "reducing a thermal expansion force and a thermal contraction force;" and "distributing a stress applied to the liquid crystal panel according to a thermal expansion of the pad part" should be construed in accordance with definitions compelled by a review of the intrinsic evidence.

D. <u>Terms or Phrases of the '121 Patent That Should Not be Construed</u>

The following terms or phrases of the '121 Patent, proposed by Defendants, should not be construed because their meanings are clear to one of ordinary skill in the art: "tape carrier package;" "output pad part;" "bent position;" "input pad part;" "not folded;" "thereby reducing a thermal expansion force and a thermal contraction force of the base film parallel to a longitudinal direction of the integrated circuit chip;" and "on the pad part."

IV. ARGUMENT

A. The Analytical Framework for Claim Construction.

In determining patent infringement, the court must first construe the scope of the patent claim as a matter of law before the fact-finder addresses the question of infringement. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Proper claim construction entails an analysis of a patent's intrinsic evidence -- *i.e.*, the claim language, the written description, and the file history. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1581-83 (Fed. Cir. 1996). The appropriate starting point, however, is necessarily with the language of the asserted claim itself. *Invitrogen Corp. v. Clonetech Labs, Inc.*, 429 F.3d 1052, 1076 (Fed. Cir. 2005). As the Federal Circuit recently confirmed, en banc, "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (citation omitted); *see also Markman*, 52 F.3d at 980 ("The written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of the claims.").

Nevertheless, it is not proper to "construe" a patent claim by changing its plain and ordinary meaning. To the contrary, construction of a claim starts with its plain language and, in the absence of some compelling reason not to, courts "must presume that the terms in the claim[s] mean what they say, and . . . . give full effect to the ordinary and accustomed meaning of claim terms." *Johnson Worldwide Assoc, Inc. v. Zebco Corp.*, 175 F.3d 985, 989 (Fed. Cir. 1999). "The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." *See Phillips*, 415 F.3d at 1313; *see also Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir.

2004) ("A court construing a patent claim seeks to accord a claim the meaning it would have to a person of ordinary skill in the art at the time of the invention.").

Courts also should not define terms that are already in simple terminology, and indeed the Federal Circuit has "question[ed] the need to consult a dictionary to determine the meaning of . . . well-known terms." *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004); *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001) (finding that trial court did not err when it declined to construe "melting" when the meaning did not depart from its ordinary meaning or otherwise require construction); *see also STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687, 698 (E.D. Tex. 2004) ("Although the [disputed] term is perhaps not simple, the individual words in the term have agreed or common meanings that are not in need of further construction."). Further, "merely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction." *C.R. Bard*, 388 F.3d at 863.

Additionally, claims "must be read in view of the specification, of which they are part." *Phillips*, 415 F.3d at 1315 (quoting *Markman*, 52 F.3d at 979). A court also looks to the specification to see whether the patentee expressly defined any of the claim terms. *See Vitronics Corp.*, 90 F.3d at 1582. "In such cases, the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316 (quoting *CCS Fitness, Inc., v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Alternatively, the specification "when read as a whole [may] suggest[] that the very character of the invention requires" limiting the ordinary meaning of a claim term. *Alloc, Inc. v. I.T.C.*, 342 F.3d 1361, 1370 (Fed. Cir. 2003); *see also Bell Atlantic Network Servs., Inc. v. Covad Communications Group*, 262 F.3d 1258, 1271 (Fed. Cir. 2001) (finding that "when a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a

single meaning, he has defined that term 'by implication'"). Nevertheless, in *Phillips*, the Federal Circuit reiterated the well-known claim construction canon that, although claims are read in light of the specification, it is improper to import limitations from the specification into the claims. *Phillips*, 415 F.3d at 1323; *see also E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1434 (Fed. Cir. 1988) (holding that the district court was wrong as a matter of law in reading extraneous limitations from the specification into the claims at issue). To emphasize this point, the court stated that "[t]o avoid importing limitations from the specification into the claims, it is important to keep in mind that the purposes of the specification are to teach and enable those of skill in the art to make and use the invention and to provide a best mode for doing so." *Phillips*, 415 F.3d at 1323.

Interpretation of patent claims will also rely upon drawings in the patents. Drawings in a specification may be used in a manner similar to the written specification to provide evidence that is highly relevant to claim interpretation. *CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1153 (Fed. Cir. 1997); *Autogiro Co. of America v. United States*, 384 F.2d 391, 398 (Cl. Ct. 1967) (noting that drawings may be used in the same manner and with the same limitations as the specification). Notably, the patent statute requires drawings "where necessary for the understanding of the subject matter [of the invention] sought to be patented." 35 U.S.C. § 113.

In addition to the specification, a court may also consider a patent's prosecution history. *Phillips*, 415 F.3d at 1317. Because the prosecution history is a record of the proceedings before the PTO, it "provides evidence of how the PTO and the inventor understood the patent." *Id.* (citing *Lemelson v. Gen. Mills, Inc.*, 968 F.2d 1202, 1206 (Fed. Cir. 1992)). The prosecution history, however, "often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Phillips*, 415 F.3d at 1317.

B. Extrinsic Evidence Is Disfavored Except under Limited Conditions.

Claims are typically interpreted solely in view of publicly available sources (*i.e.*, the intrinsic evidence), and consideration of extrinsic evidence during claim construction is generally disfavored. *Vitronics*, 90 F.3d at 1583. Indeed, the *Phillips* court cautioned that extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language" and may not be "used to contradict claim meaning that is unambiguous in light of the intrinsic evidence." *Phillips*, 415 F.3d at 1317, 1324 (internal quotation omitted); *see also Pfizer Inc. v. Ranbaxy Labs. Ltd.*, 405 F. Supp. 2d 495, 502 (D. Del. 2005) (noting that "extrinsic evidence is considered less reliable and less useful in claim construction than the patent and its prosecution history." (citing *Phillips,* 415 F.3d at 1318-19)). Accordingly, "[i]n those cases where the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Vitronics*, 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324 (reaffirming approach to claim construction outlined in *Vitronics*).

C. Proper Construction of the Terms and Phrases of the '002 Patent in Dispute

1. Terms and Phrases of the '002 Patent That Should Be Construed

a. "interconnecting" (Claims 1 and 12)

Although the term "interconnecting" has more than one ordinary meaning, the proper construction of the term is "shorting," because "interconnecting" was used throughout the entire ~~intrinsic record in a manner consistent with this single meaning. *Bell Atlantic*, 262 F.3d at 1271.~~

Turning first to the claims, the term "interconnecting" in the context of claims 1 and 12 refers to interconnecting substantially all of the row lines to one another, and substantially all of the column lines to one another. The portion of the specification that corresponds to this claim

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language unmistakably supports the construction of "interconnecting" as "shorting." Indeed, the specification explicitly states the following:

> The bus [column] lines 82 and 86 are interconnected *(shorted)* at or before the pad 84 and are interconnected *(shorted)* at the opposite ends by a line or short 88. . . .
>
> The bus [row] lines 90 and 94 are interconnected *(shorted)* at or before the pad 92 and are interconnected *(shorted)* at the opposite ends by a line or short 96.

Ex. A, the '002 Patent, at col. 5, l. 65 - col. 6, l. 9 (emphasis added).

Turning next to the prosecution history, nothing in the prosecution history of the '002 Patent contradicts the definition of "shorting" as the ordinary meaning of the term "interconnecting."

Finally, because the publicly available intrinsic record unambiguously defines the scope of the term, any reliance on extrinsic evidence is improper. *See Vitronics Corp.*, 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324. For all of these reasons, the term "interconnecting" is properly construed as "shorting" in claims 1 and 12 of the '002 Patent.

In contrast, Defendants' proposed construction of "electrically connecting" is not supported by the intrinsic record, and should be rejected by this Court.

b. "resistance" (Claims 1, 2, 3, and 12-14)

The term "resistance" has an ordinary meaning of "any component used to cause a voltage drop during current flow." As explained below, all of the intrinsic sources of claim construction support this ordinary meaning, and the term should be so construed.

It is well-known to one of ordinary skill in the art that "resistance" is an intrinsic characteristic of materials and devices. Resistance is a measure of the materials' or devices' opposition to the flow of electric current. All circuit components, regardless of whether the component is a resistor, diode, or transistor, have the characteristic of resistance. The intrinsic

evidence is consistent with this universal understanding in the art, and discloses that semiconductor materials, such as those used to form diodes and transistors, have a measurable value of resistance. For example, the specification suggests that one way to overcome damage to gate material of a thin film transistor is to make the gate material very thin, but acknowledges that a transistor with such a thin gate could not be used in large transistor arrays necessary for LCD backplanes because "the resistivity is then too high." Ex. A, the '002 Patent, at col. 4, ll. 32-34.

In contrast, Defendants' lengthy construction of "resistance" is contrived to narrow the scope of this simple and straightforward claim term. Specifically, Defendants' construction attempts to improperly equate "resistance" with "resistor:"

> "A resistance, as it is used in the claims, means a resistor, which is an electric circuit element that has a specified resistance to the flow of electrical current. A resistance does not include switching elements such as transistors and diodes.

There is no support for Defendants' position that switching elements, such as transistors and diodes, do not provide a resistance to electrical current; as such, this construction should be rejected.

c. "pickup pad" (Claims 3, 4, 6, 14, 15, 17 and 35)

When properly construed, the term "pickup pad" is "a conductive area used to electrically connect the back plane to the front plane."

The term "pickup pad" is disclosed in the specification for electrically connecting the back plane to the front plane:

> A backplane pickup contact pad 216 also is provided, which includes a corner 218 for aligning the backplane with the front plane. The pad 216 includes a shunt line 220 which is connected to one set of source or gate lines via a shunt transistor 222 along the edge to be scribed and removed along the line 206. . . . There will be at least one corner backplane pickup pad 216 and

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> preferably there will be two or three, each with their associated shunt transistors.

Ex. A, the '002 Patent, at col. 8, ll. 18-39; *see also* Fig. 7.

One of ordinary skill in the art would understand the term "pad" to be a conductive area. The pickup pad "picks up" the voltage between the back plane and the front plane, thereby electrically connecting the back plane to the front plane. The prosecution history is consistent with this construction; as such, any reliance on extrinsic evidence is improper. *See Vitronics Corp.*, 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324.

LPL's proposed definition is in accordance with the meaning of "pick up pad" to one of ordinary skill in the art. The pickup pad, described in the specification and depicted in Figure 7, is consistent with LPL's construction. In contrast, Defendants' proposed construction of "pickup pad" as "a pad located at the corner region of a backplane for *aligning* the frontplane and backplane" ignores the fact that the pickup pad is used to electrically connect these glass substrates.

d. "shunt switching element" (Claims 3, 4, 8, 9, 14 and 15)

The term "shunt switching element" has an ordinary meaning of "a parallel switching device." As explained below, all of the intrinsic sources of claim construction necessitate this ordinary meaning, and the Court should adopt this construction.

Turning first to the claim language, it is clear that shunt switching elements are devices that couple various elements within the circuit. Specifically, they couple the pickup pad to the resistance. *See, e.g.*, Ex. A, the '002 Patent, claims 2-4. Additionally, shunt switching elements couple the inner electrostatic discharge guard ring to the row and column lines. *See, e.g.*, Ex. A, the '002 Patent, claim 8.

The specification clearly supports that a switching element includes devices such as transistors or optionally diodes, *i.e.*, switching devices. Throughout the specification, "switching element" refers to a device such as a transistor or diode. For example, the specification discloses "a switching element, transistor 22 . . . ." Ex. A, the '002 Patent, at col. 3, ll. 48-49; and col. 4, ll. 10-11. Additionally, the specification states that "the shunt transistors 146, 194 and 222, etc. also can be formed as other active switching elements, such as diodes." Ex. A, the '002 Patent, at col. 8, ll. 57-59.

The word "shunt" is used throughout the specification to indicate those elements that are connected in parallel with the protected circuit. In describing the connection between the pickup pad and the row and column lines, and the outer electrostatic discharge guard ring, the specification refers to that portion of the circuitry as composed of "shunt line 220," "shunt transistor 222," "shunt line 224," and "shunt transistor 226." Ex. A, the '002 Patent, at col. 8, ll. 20-26. As shown in Figure 7 of the '002 patent, the pickup pad is connected in parallel with the protected circuit. Furthermore, "shunt transistors 22," coupling the inner electrostatic discharge guard ring to the row and column lines, are arranged in parallel with respect to the protected circuit. *See*, *e.g.*, Ex. A, the '002 Patent, Figure 5.

The prosecution history is also consistent with LPL's construction. During prosecution, the Examiner addressed the "shunt switching means," citing to U.S. Patent 4,736,271 (hereinafter "the '271 Patent"). The '271 Patent discloses the use of diodes as shunt elements. *See*, *e.g.,* Ex. I, the '271 Patent, col. 4, ll. 66-68. These shunt elements are also disclosed as being connected in parallel with respect to the protected circuit. *See*, *e.g.*, Ex. I, the '271 Patent, Figures 3, and 6-7.

The language of the claims, the specification, and the prosecution history clearly shows that the proper construction of "shunt switching element" is "parallel switching device," which is the ordinary meaning of the term as understood by one of ordinary skill in the art at the time of the invention. As such, any reliance on extrinsic evidence is improper. *See Vitronics* Corp., 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324.

In contrast, Defendants' proposed construction of "a device that is capable of switching between on and off states (*e.g.*, a transistor or diode) to open or close a by-pass for diverting electrical current" is unclear and not supported by the intrinsic record. Defendants' construction improperly limits the meaning of the term to a device capable only of switching between states. Neither the specification, nor the claims, nor the prosecution history supports limiting the term in this manner. As stated above, the specification expressly refers to the use of transistors, *i.e.*, devices that can control the amount of current through them, and it only references the use of diodes as a possible modification.

Further, the device necessarily must be a parallel device, yet Defendants' proposed construction fails to address this critical feature. At best, "to open or close a by-pass for diverting electrical current" suggests an element that connects to an unspecified secondary circuit. There no relationship between this unclear definition and the word "shunt."

Accordingly, this Court should adopt LPL's proposed construction of "parallel switching device" and reject Defendants' proposed construction.

e. "outer electrostatic discharge guard ring" (Claim 1, 2, 7, 12, 13, 18)

The intrinsic record makes clear that the term "outer electrostatic discharge guard ring" is properly construed as "a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."

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Turning first to the claim language, and in fact focusing on the disputed term itself, it is an *outer ring* to *guard* against, or to provide protection from, *electrostatic discharges*. Indeed, claim 1 explicitly recites that the outer electrostatic discharge guard ring "provide[s] protection from electrostatic discharges."

Next, the specification clearly supports both that: (1) the guard ring can be a closed or open ring, or open L or C-shaped line; and (2) the outer guard ring is outside the active matrix display. First, with regard to the shape of a guard ring, the specification explicitly states that, although the guard ring 144 (in this case, the inner guard ring), is illustrated as a closed ring, it could also be "an open L or C-shaped line." Ex. A, the '002 Patent, at col. 7, ll. 18-20. Second, with regard to the "outer" location of the guard ring, the specification discloses that "the outer guard ring 200 is connected to all of one of the source and gate pads (not illustrated) . . . ." *Id.* at col. 8, ll. 5-6. It would be clear to one of ordinary skill in the art, especially in view of Figure 1, that the source and gate pads are on the outside of the active matrix display. The prosecution history is also consistent with this construction and, as such, any reliance on extrinsic evidence is improper. *See Vitronics Corp.*, 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324.

In contrast, Defendants' proposed construction of "a ring of conductor, located external to the inner electrostatic discharge guard ring if the two rings are used together, for draining off static buildup to prevent electrostatic discharge" is clearly not supported by the intrinsic record. It is indisputable that the outer electrostatic discharge guard ring *cannot* drain off static buildup to prevent electrostatic discharge. One of ordinary skill in the art would understand, and the intrinsic record makes clear, that electrostatic discharge cannot be *prevented*, and, as such, the guard rings serve to provide *protection from*, *not prevention of*, electrostatic discharges. *See*,

e.g., Ex. A, the '002 Patent at col. 1, ll. 2-3; col. 2, ll. 40-41; col. 7, ll. 41-42; and col. 8, l. 28 ("The outer ESD guard ring 200 provides ESD protection.").

Accordingly, this Court should reject Defendants' construction of the term "outer electrostatic discharge guard ring" and adopt LPL's proposed construction of "a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."

f. "inner electrostatic discharge guard ring" (Claim 8)

It is clear from the intrinsic record that the term "inner electrostatic discharge guard ring" is properly construed as "a closed or open ring, or open L or C-shaped line, inside the outer guard ring to provide protection from electrostatic discharges."

Turning first to the claim language, and in fact focusing on the disputed term itself, it is an *inner ring* to *guard* against, or provide protection from, *electrostatic discharges*. Indeed, claim 8 explicitly recites that the inner electrostatic discharge guard ring "provide[s] protection from electrostatic discharges."

Next, the specification clearly supports both that: (1) the guard ring can be a closed or open ring, or open L or C-shaped line; and (2) the inner guard ring is inside the outer guard ring. First, with regard to the shape of a guard ring, the specification clearly states that, "the guard ring 144 [the inner guard ring] is illustrated as a closed ring, but could also be an open L or C-shaped line . . . ." Ex. A, the '002 Patent, at col. 7, ll. 18-20. Second, with regard to the relative locations of the guard rings, the specification repeatedly refers to the inner guard ring as being "internal" and to the outer guard ring as being "external." *See*, *e.g.*, Ex. A, the '002 Patent, at col. 2, ll. 54-69.

The prosecution history also supports the relative positions of the inner and outer guard rings. Specifically, to distinguish over the prior art, the Applicant highlighted the novel

relationship between the inner and outer electrostatic discharge guard rings by emphasizing that a "*dual ring* is not suggested by any of the references alone or combined." Ex. G, Proposed Response filed July 2, 1990, at p. 2 (emphasis added).

Finally, because the publicly available intrinsic record unambiguously defines the scope of the term, any reliance on extrinsic evidence is improper. *See Vitronics Corp.*, 90 F.3d at 1583; *see also Phillips*, 415 F.3d at 1324.

In contrast, Defendants' proposed construction of "a ring of conductor, located internal to the outer electrostatic discharge guard ring, for draining off electrostatic buildup to prevent electrostatic discharge" is not supported by the intrinsic record. It is indisputable that the inner electrostatic discharge guard ring *cannot* drain off electrostatic buildup to prevent electrostatic discharge. One of ordinary skill in the art would understand, and the intrinsic record makes clear, that electrostatic discharge cannot be *prevented*, and, as such, the guard rings serve to provide *protection from*, *not prevention of*, electrostatic discharges. *See*, *e.g.*, Ex. A, the '002 Patent at col. 2, ll. 52-57.

Accordingly, this Court should reject Defendants' construction of the term "inner electrostatic discharge guard ring" and adopt LPL's proposed construction of "a closed or open ring, or open L or C-shaped line, inside the outer electrostatic discharge ring to provide protection from electrostatic discharges."

2. Terms and Phrases of the '002 Patent That Should Not Be Construed

a. "interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another" (Claim 1 and 12)

The phrase "interconnecting substantially all of said row lines to one another *and* substantially all of said column lines to one another" does not need construction. If a construction of this phrase must be made, however, it should not be given Defendants' proposed

construction, which not only inexplicably separates the phrase into two separate phrases, but construes the separated phrases to artificially narrow the scope of LPL's patent protection.

Specifically, Defendants construe "interconnecting substantially all of said row lines to one another" to mean "electrically connecting by conductors all, or nearly all, of row lines to one another"; and separately construe "interconnecting . . . substantially all of said column lines to one another" to mean "electrically connecting by conductors all, or nearly all, of column lines to one another." Given that Defendants appear to be construing the phrases identically, their separation is nonsensical and unnecessary. More importantly, however, Defendants' narrow construction is not supported by the intrinsic record. First, nowhere in the specification is "interconnecting" limited to "electrically connecting by conductors." As discussed above, the specification explicitly recites that the row lines and column lines are "interconnected (*shorted*)" to one another. Ex. A, the '002 Patent, at col. 5, l. 65 - col. 6, l. 9 (emphasis added). Second, Defendants also construe, albeit without support, "substantially all" to mean "all, or nearly all." The specification, however, does not require this construction; rather, the specification discloses that the interconnection of the row lines and column lines be sufficient to provide protection from electrostatic discharge. *See, e.g.*, Ex. A, the '002 Patent at col. 6, ll. 26-59. Furthermore, such a construction goes against the open-ended claim format selected by LPL for the '002 Patent (*e.g.*, "comprising . . ."). Thus, the construction of "interconnecting substantially all of said row lines to one another *and* substantially all of said column lines to one another" should be construed in accordance with the ordinary meaning.

Accordingly, to the extent any construction is necessary, the ordinary meaning of this phrase to one of ordinary skill in the art should apply, and "interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another " should be

construed as "sufficiently interconnecting said row lines to one another and said columns lines to one another to provide protection from electrostatic discharge."

b. "electrostatic discharges" (Claims 1, 8, 12)

The term "electrostatic discharges" is simple, clear, and does not require construction. If a construction of this term must be made, however, it should not be given Defendants' proposed construction of "flow of electrical current caused by a build-up of static electrical charges," which only adds ambiguity to an otherwise straightforward term universally understood in the art. For example, the term "build-up" implies that electrostatic discharges must accumulate gradually over time, yet one of ordinary skill would clearly understand that such may not be the case. Nor is this artificial restriction supported by the intrinsic record. *See, e.g.*, Ex. A, the '002 Patent at col. 4, ll. 46-49 ("[e]lectrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20."). Moreover, Defendants' proposed construction of "flow" could require steady, smooth, and free passage of electricity. One of ordinary skill in the art would understand that electrostatic discharges do not necessarily "flow." Lightning is an example of an electrostatic discharge that happens suddenly. The electrical current passes suddenly from one place to another, *i.e.*, from the sky to the earth. For a TFT transistor, the electrical charge on a source terminal of a transistor passes suddenly to the gate terminal; it is neither a gradual flow nor a "draining off," as Defendants suggest.

To the extent construction of the term "electrostatic discharges" is necessary, the plain and ordinary meaning of this term should apply, and "electrostatic discharges" should be construed as "a release of current resulting from a voltage differential caused by static electricity."

c. "coupled to said interconnected row and column lines via a resistance" (Claims 1 and 12)

The phrase "coupled to said interconnected row and column lines via a resistance" does not need construction. The meaning of the term "coupled" is plain on its face. If a construction of this phrase must be made, however, it should not be given Defendants' proposed construction of "linked through one or more resistors to the interconnected column lines and the interconnected row lines." First, as discussed above, Defendants improperly limit the term "resistance," to a single type of component: a resistor. Second, by limiting the term "coupled" to require linking through one or more resistors, Defendants have defined "coupled" even *more narrowly* than they have defined "interconnecting," which Defendants have construed as "electrically connecting." It is indisputable that one of ordinary skill in the art would understand that the reverse is true, and that the intrinsic record of the '002 Patent does nothing to alter the ordinary meaning of the word "coupled."

In view of the foregoing, the phrase "coupled to said interconnected row and column lines via a resistance," which uses commonly understood words and, therefore, should be given its ordinary meaning, *see Phillips*, 415 F.3d at 1313, is properly construed as "electrically connected to said interconnected row and column lines via a resistance."

d. "removing said outer guard ring and row and column interconnections" (Claims 1 and 12)

In its proper context, the meaning of the phrase "removing said outer guard ring and row and column interconnections" does not require construction. If a construction of this phrase must be made, however, it should not be given Defendants' proposed construction of "electrically disconnecting the interconnections between rows and between columns and disconnecting rows and columns from the outer guard ring." This construction is not supported

by the plain meaning of the phrase, and is contradicted by the claim language and the specification.

In effect, Defendants are impermissibly treating the claim terms as "a nose of wax," for example, by construing the *same* occurrence of the term "removing" to mean both "electrically disconnecting" and "disconnecting." Such a construction cannot stand.

The meaning of the term "removing" is plain on its face and does not require construction. To the extent any construction is necessary, the plain and ordinary meaning of this term should apply and "removing said outer guard ring and row and column interconnections prior to completion of the display" should be construed as "physically disconnecting said guard ring and row and column interconnections."

e. "corner pad" (Claims 7 and 18)

In its proper context, the meaning of the term "corner pad" does not require construction. If a construction of this term must be made, however, it should not be given Defendants' proposed construction of "a pad of metal or other conductive materials that is located at the corner of an outer guard ring, and electrically connected with the outer ring." Such a construction is untenable in view of claim language alone.

Specifically, the claim language (claims 7 and 18) explicitly recites that the corner pad is formed "on at least one corner of the *display*," and not at a "corner of the outer guard ring." Moreover, the corner pad is not "electrically connected with the outer guard ring," but rather is formed, and "align[ed] [with] scribe lines . . . for *removing* said outer guard ring."

To the extent construction of the term "corner pad" is necessary, the plain and ordinary meaning to one of ordinary skill in the art should apply, and "corner pad" should be construed as "a reference mark for cutting."

f. "scribe line" (Claims 7 and 18)

The meaning of the term "scribe line" is plain on its face and does not require construction. If a construction of this term must be made, however, it should not be given Defendants' proposed construction of "a predefined line along which the glass substrate can be marked with a sharp tool either to disconnect the conductor patterns along the line or to initiate the fracture of the glass substrate along the line." Such a construction is not supported by the intrinsic record and is clearly contrived to narrow artificially the scope of a simple and straightforward claim term.

To the extent any construction is necessary, the plain and ordinary meaning of should apply, and "scribe line" should be construed to mean "cutting line based on reference marks."

g. "aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections" (Claims 7 and 18)

The phrase "aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections" does not require construction. If a construction of this phrase must be made, however, it should not be given Defendants' proposed construction of "aligning each scribe line with one edge of the corner pad for removing the outer guard ring and row and column interconnections." Among other things, Defendants fail to construe "aligning," which is the only claim term first introduced in the proposed phrase. The reason for Defendants' apparent oversight is clear: to narrow improperly, without any basis whatsoever in the intrinsic record, the term "said corner pad" to mean "one edge of the corner pad." Such a construction cannot stand.

The meaning of the term "aligning" is plain on its face and does not require construction. To the extent any construction is necessary, the plain and ordinary meaning of this term should apply and "aligning" should mean "adjusting."

The meaning of the phrase "on the pad part" is plain on its face and does not require construction. To the extent any construction is necessary, the plain and ordinary meaning of this phrase should apply, and "on the part" should be construed as "at or along, or in proximity to, the pad part."

V. CONCLUSION

For all of the foregoing reasons, LPL submits that the Court construe the above disputed phrases in accordance with LPL's proposed constructions.

March 8, 2006

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CERTIFICATE OF SERVICE

The undersigned counsel certifies that, on March 8, 2006, he electronically filed the foregoing document with the Clerk of the Court using CM/ECF, which will send automatic notification of the filing to the following:

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EXHIBIT B-4

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

LG. PHILIPS LCD CO. LTD,	:	
Plaintiff,	:	
v.	:	Civil Action No. 05-292-JJF
TATUNG COMPANY, TATUNG COMPANY OF AMERICA, INC., CHUNGWHA PICTURE TUBES LTD., and VIEWSONIC CORP.,	:	
Defendants.	:	

O R D E R

At Wilmington, this 13 Day of June, 2006, for the reasons set forth in the Memorandum Opinion issued this date,

IT IS HEREBY ORDERED that for the purposes of United States Patent No. 6,738,121, the following terms and phrases are construed as follows:

1. The term "**interconnecting**," as used in claim 1, means "electrically connecting with conductors;"

2. The phrase "**removing said outer guard ring and row and column interconnections**," as used in claims 1 and 12, means "physically disconnecting said guard ring and row and column interconnections;"

3. The term "**outer electrostatic discharge guard ring,**" as used in claims 12, 19, and 30, means "a closed or open ring, or

open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges;"

4. The term "**resistance**," as used in claims 1, 2, 3, 12, 13, 14, 19, 20, 21, 30, 31, and 32, means "a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from electrostatic discharge;"

5. The term "**corner pad**," as used in claims 7, 18, 25, and 36, means "an area of conductive material;"

6. The Court declines to construe the term "**pickup pad**."

Joseph J Farnan Jr

UNITED STATES DISTRICT JUDGE

EXHIBIT B-5

Merriam-Webster's Collegiate® Dictionary

TENTH EDITION

Merriam-Webster, Incorporated
Springfield, Massachusetts, U.S.A.

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Abbı

QUIOUS implies fawning or sycophantic compliance and exaggerated deference of manner ⟨waiters who are *obsequious* in the presence of celebrities⟩.

sub·set \'səb-,set\ *n* (1902) **:** a set each of whose elements is an element of an inclusive set

sub·shrub \-,shrəb, *esp Southern* -,srəb\ *n* (1851) **:** a perennial plant having woody stems except for the terminal part of the new growth which is killed back annually; *also* **:** a low shrub

sub·side \səb-'sīd\ *vi* **sub·sid·ed; sub·sid·ing** [L *subsidere,* fr. *sub-* + *sidere* to sit down, sink; akin to L *sedēre* to sit — more at SIT] (1607) **1 :** to sink or fall to the bottom **:** SETTLE **2 :** to tend downward **:** DESCEND; *esp* **:** to flatten out so as to form a depression **3 :** to let oneself settle down **:** SINK ⟨*subsided* into a chair⟩ **4 :** to become quiet or less ⟨as the fever ~*s*⟩ ⟨my anger *subsided*⟩ *syn* see ABATE — **sub·si·dence** \səb-'sī-dᵊn(t)s, 'səb-sə-dən(t)s\ *n*

sub·sid·i·ar·i·ty \,səb-si-dē-'er-ə-tē, səb-,si-\ *n* (1936) **1 :** the quality or state of being subsidiary **2 :** a principle in social organization: functions which subordinate or local organizations perform effectively belong more properly to them than to a dominant central organization

¹sub·sid·i·ary \səb-'si-dē-,er-ē, -'si-də-rē\ *adj* [L *subsidiarius,* fr. *subsidium* reserve troops] (1543) **1 a :** furnishing aid or support **:** AUXILIARY ⟨~ details⟩ **b :** of secondary importance ⟨a ~ stream⟩ **2 :** of, relating to, or constituting a subsidy ⟨a ~ payment to an ally⟩ — **sub·sid·i·ari·ly** \-,si-dē-'er-ə-lē\ *adv*

²subsidiary *n, pl* **-ar·ies** (1603) **:** one that is subsidiary; *esp* **:** a company wholly controlled by another

sub·si·dise *Brit var of* SUBSIDIZE

sub·si·dize \'səb-sə-,dīz, -zə-\ *vt* **-dized; -diz·ing** (1795) **:** to furnish with a subsidy: as **a :** to purchase the assistance of by payment of a subsidy **b :** to aid or promote (as a private enterprise) with public money ⟨~ soybean farmers⟩ ⟨~ public transportation⟩ — **sub·si·di·za·tion** \,səb-sə-də-'zā-shən, -zə-\ *n* — **sub·si·diz·er** *n*

sub·si·dy \'səb-sə-dē, -zə-\ *n, pl* **-dies** [ME, fr. L *subsidium* reserve troops, support, assistance, fr. *sub-* near + *sedēre* to sit — more at SUB-, SIT] (14c) **:** a grant or gift of money: as **a :** a sum of money formerly granted by the British Parliament to the crown and raised by special taxation **b :** money granted by one state to another **c :** a grant by a government to a private person or company to assist an enterprise deemed advantageous to the public

sub·sist \səb-'sist\ *vb* [LL *subsistere* to exist, fr. L, to come to a halt, remain, fr. *sub-* + *sistere* to come to a stand; akin to L *stare* to stand — more at STAND] *vi* (1549) **1 a :** to have existence **:** BE **b :** PERSIST, CONTINUE **2 :** to have or acquire the necessities of life (as food and clothing); *esp* **:** to nourish oneself ⟨~*ing* on roots, berries and grubs⟩ **3 a :** to hold true **b :** to be logically conceivable as the subject of true statements ~ *vt* **:** to support with provisions

sub·sis·tence \səb-'sis-tən(t)s\ *n* [ME, fr. LL *subsistentia,* fr. *subsistent-, subsistens,* prp. of *subsistere*] (15c) **1 a (1) :** real being **:** EXISTENCE **(2) :** the condition of remaining in existence **:** CONTINUATION, PERSISTENCE **b :** an essential characteristic quality of something that exists **c :** the character possessed by whatever is logically conceivable **2 :** means of subsisting: as **a :** the minimum (as of food and shelter) necessary to support life **b :** a source or means of obtaining the necessities of life — **sub·sis·tent** \-tənt\ *adj*

subsistence farming *n* (1939) **1 :** farming or a system of farming that provides all or almost all the goods required by the farm family usu. without any significant surplus for sale **2 :** farming or a system of farming that produces a minimum and often inadequate return to the farmer — called also *subsistence agriculture* — **subsistence farmer** *n*

sub·so·cial \,səb-'sō-shəl\ *adj* (ca. 1909) **:** incompletely social; *esp* **:** tending to associate gregariously but lacking fixed or complex social organization ⟨~ insects⟩

¹sub·soil \'səb-,sȯil\ *n* (1799) **:** the stratum of weathered material that underlies the surface soil

²subsoil *vt* (1840) **:** to turn, break, or stir the subsoil of — **sub·soil·er** *n*

sub·so·lar point \,səb-'sō-lər-\ *n* (ca. 1908) **:** the point on the surface of the earth or a planet at which the sun is at the zenith

sub·son·ic \,səb-'sä-nik\ *adj* [ISV] (1937) **1 :** of, relating to, or being a speed less than that of sound in air **2 :** moving, capable of moving, or utilizing air currents moving at a subsonic speed **3 :** INFRASONIC 1 — **sub·son·i·cal·ly** \-ni-k(ə-)lē\ *adv*

sub·space \'səb-,spās\ *n* (1927) **:** a subset of a space; *esp* **:** one that has the essential properties (as those of a vector space or topological space) of the including space

sub spe·cie ae·ter·ni·ta·tis \sub-'spe-kē-,ā-,ī-,ter-nə-'tä-təs\ *adv* [NL, lit., under the aspect of eternity] (1895) **:** in its essential or universal form or nature

sub·spe·cies \'səb-,spē-shēz, -sēz\ *n* [NL] (1699) **:** a subdivision of a species: as **a :** a category in biological classification that ranks immediately below a species and designates a population of a particular geographical region genetically distinguishable from other such populations of the same species and capable of interbreeding successfully with them where its range overlaps theirs **b :** a named subdivision (as a race or variety) of a taxonomic species **c :** SUBGROUP 1 ⟨~ of economy fares —Michael DiPaola⟩ — **sub·spe·cif·ic** \,səb-spi-'si-fik\ *adj*

sub·stage \'səb-,stāj\ *n* (1888) **:** an attachment to a microscope by means of which accessories (as mirrors, diaphragms, or condensers) are held in place beneath the stage of the instrument

sub·stance \'səb-stən(t)s\ *n* [ME, fr. MF, fr. L *substantia,* fr. *substant-, substans,* prp. of *substare* to stand under, fr. *sub-* + *stare* to stand — more at STAND] (14c) **1 a :** essential nature **:** ESSENCE **b :** a fundamental or characteristic part or quality **c** *Christian Science* **:** GOD 1b **2 a :** ultimate reality that underlies all outward manifestations and change **b :** practical importance **:** MEANING, USEFULNESS ⟨the . . . bill—which will be without ~ in the sense that it will authorize nothing more than a set of ideas —Richard Reeves⟩ **3 a :** physical material from which something is made or which has discrete existence **b :** matter of particular or definite chemical constitution **c :** something (as drugs or alcoholic beverages) deemed harmful and usu. subject to legal restriction ⟨possession of a controlled ~⟩ ⟨has a ~ problem⟩ **4 :** material possessions **:** PROPERTY ⟨a family of ~⟩ — **sub·stance·less** \-ləs\ *adj* — **in substance :** in respect to essentials **:** FUNDAMENTALLY

substance abuse *n* (1982) **:** excessive use of a drug (as alcohol, narcotics, or cocaine) **:** use of a drug without medical justification — **substance abuser** *n*

substance P *n* (1934) **:** a neuropeptide that consists of 11 amino-acid residues, that is widely distributed in the brain, spinal cord, and peripheral nervous system, and that acts across nerve synapses to produce prolonged postsynaptic excitation

sub·stan·dard \,səb-'stan-dərd\ *adj* (1897) **:** deviating from or falling short of a standard or norm: as **a :** of a quality lower than that prescribed by law **b :** conforming to a pattern of linguistic usage existing within a speech community but not that of the prestige group in that community **c :** constituting a greater than normal risk to an insurer

sub·stan·tial \səb-'stan(t)-shəl\ *adj* (14c) **1 a :** consisting of or relating to substance **b :** not imaginary or illusory **:** REAL, TRUE **c :** IMPORTANT, ESSENTIAL **2 :** ample to satisfy and nourish **:** FULL ⟨a ~ meal⟩ **3 a :** possessed of means **:** WELL-TO-DO **b :** considerable in quantity **:** significantly great ⟨earned a ~ wage⟩ **4 :** firmly constructed **:** STURDY **5 :** being largely but not wholly that which is specified ⟨a ~ lie⟩ — **substantial** *n* — **sub·stan·ti·al·i·ty** \-,stan(t)-shē-'a-lə-tē\ *n* — **sub·stan·tial·ly** \-'stan(t)-sh(ə-)lē\ *adv* — **sub·stan·tial·ness** \-'stan(t)-shəl-nəs\ *n*

sub·stan·tia ni·gra \səb-,stan(t)-shē-ə-'nī-grə, -'ni-\ *n, pl* **sub·stan·ti·ae ni·grae** \-chē-,ē-'nī-(,)grē, -'ni-\ [NL, lit., black substance] (1882) **:** a layer of deeply pigmented gray matter situated in the midbrain and containing the cell bodies of a tract of dopamine-producing nerve cells whose secretion tends to be deficient in Parkinson's disease

sub·stan·ti·ate \səb-'stan(t)-shē-,āt\ *vt* **-at·ed; -at·ing** (1657) **1 :** to give substance or form to **:** EMBODY **2 :** to establish by proof or competent evidence **:** VERIFY ⟨~ a charge⟩ *syn* see CONFIRM — **sub·stan·ti·a·tion** \-,stan(t)-shē-'ā-shən\ *n* — **sub·stan·ti·a·tive** \-'stan(t)-shē-,ā-tiv\ *adj*

sub·stan·ti·val \,səb-stən-'tī-vəl\ *adj* (ca. 1832) **:** of, relating to, or serving as a substantive — **sub·stan·ti·val·ly** \-və-lē\ *adv*

¹sub·stan·tive \'səb-stən-tiv\ *n* [ME *substantif,* fr. MF, fr. *substantif,* adj., having or expressing substance, fr. LL *substantivus*] (14c) **:** NOUN; *broadly* **:** a word or word group functioning syntactically as a noun — **sub·stan·tiv·ize** \-ti-,vīz\ *vt*

²sub·stan·tive \'səb-stən-tiv; *2c & 3 also* səb-'stan-tiv\ *adj* [ME, fr. LL *substantivus* having substance, fr. L *substantia*] (14c) **1 :** being a totally independent entity **2 a :** real rather than apparent **:** FIRM; *also* **:** PERMANENT, ENDURING **b :** belonging to the substance of a thing **:** ESSENTIAL **c :** expressing existence ⟨the ~ verb is the verb *to be*⟩ **d :** requiring or involving no mordant ⟨a ~ dyeing process⟩ **3 a :** having the nature or function of a grammatical substantive ⟨a ~ phrase⟩ **b :** relating to or having the character of a noun or pronominal term in logic **4 :** considerable in amount or numbers **:** SUBSTANTIAL **5 :** creating and defining rights and duties ⟨~ law⟩ — compare PROCEDURAL **6 :** having substance **:** involving matters of major or practical importance to all concerned ⟨~ discussions among world leaders⟩ — **substan·tive·ly** *adv* — **sub·stan·tive·ness** *n*

substantive due process *n* (1954) **:** DUE PROCESS 2

substantive right *n* (1939) **:** a right (as of life, liberty, property, or reputation) held to exist for its own sake and to constitute part of the normal legal order of society

sub·sta·tion \'səb-,stā-shən\ *n* (1881) **:** a subordinate or subsidiary station: as **a :** a branch post office **b :** a subsidiary station in which electric current is transformed **c :** a police station serving a particular area

sub·stit·u·ent \səb-'sti-chə-wənt, -'stich-wənt\ *n* [L *substituent-, substituens,* prp. of *substituere*] (ca. 1896) **:** an atom or group that replaces another atom or group in a molecule — **substituent** *adj*

sub·sti·tut·able \'səb-stə-,tü-tə-bəl, -'tyü-\ *adj* (1805) **:** capable of being substituted — **sub·sti·tut·abil·i·ty** \,səb-stə-,tü-tə-'bi-lə-tē, -,tyü-\ *n*

¹sub·sti·tute \'səb-stə-,tüt, -,tyüt\ *n* [ME, fr. L *substitutus,* pp. of *substituere* to put in place of, fr. *sub-* + *statuere* to set up, place — more at STATUTE] (15c) **:** a person or thing that takes the place or function of another — **substitute** *adj*

²substitute *vb* **-tut·ed; -tut·ing** *vt* (1588) **1 a :** to put or use in the place of another **b :** to introduce (an atom or group) as a substituent; *also* **:** to alter (as a compound) by introduction of a substituent ⟨a *substituted* benzene ring⟩ **2 :** to take the place of **:** REPLACE ~ *vi* **:** to serve as a substitute

sub·sti·tu·tion \,səb-stə-'tü-shən, -'tyü-\ *n* [ME *substitucion,* fr. MF *substitution,* fr. LL *substitution-, substitutio,* fr. *substituere*] (14c) **1 a :** the act, process, or result of substituting one thing for another **b :** replacement of one mathematical entity by another of equal value **2 :** one that is substituted for another — **sub·sti·tu·tion·al** \-shnəl, -shə-nᵊl\ *adj* — **sub·sti·tu·tion·al·ly** *adv* — **sub·sti·tu·tion·ary** \-shə-,ner-ē\ *adj*

substitution cipher *n* (1936) **:** a cipher in which the letters of the plaintext are systematically replaced by substitute letters — compare TRANSPOSITION CIPHER

sub·sti·tu·tive \'səb-stə-,tü-tiv, -,tyü-\ *adj* (1668) **:** serving or suitable as a substitute — **sub·sti·tu·tive·ly** *adv*

sub·strate \'səb-,strāt\ *n* [ML *substratum*] (1807) **1 :** SUBSTRATUM **2 :** the base on which an organism lives ⟨the soil is the ~ of most seed plants⟩ **3 :** a substance acted upon (as by an enzyme)

sub·stra·tum \'səb-,strā-təm, -,stra-, ,səb-'\ *n, pl* **-stra·ta** \-tə\ [ML, fr. L, neut. of *substratus,* pp. of *substernere* to spread under, fr. *sub-* + *sternere* to spread — more at STREW] (1631) **:** an underlying support **:** FOUNDATION: as **a :** substance that is a permanent subject of qualities or phenomena **b :** the material of which something is made and from which it derives its special qualities **c :** a layer beneath the surface soil; *specif* **:** SUBSOIL **d :** SUBSTRATE 2

sub·struc·ture \'səb-,strək-chər\ *n* (1726) **:** an underlying or supporting part of a structure — **sub·struc·tur·al** \-chə-rəl, -shrəl\ *adj*

sub·sume \səb-'süm\ *vt* **sub·sumed; sub·sum·ing** [NL *subsumere,* fr. L *sub-* + *sumere* to take up — more at CONSUME] (1825) **:** to include or place within something larger or more comprehensive **:** encompass as a subordinate or component element ⟨red, green, and yellow are *subsumed* under the term "color"⟩ — **sub·sum·able** \-'sü-mə-bəl\ *adj*

sub·sump·tion \səb-'səm(p)-shən\ *n* [NL *subsumption-, subsumptio,* fr. *subsumere*] (1651) **:** the act or process of subsuming

EXHIBIT C-2

Office Action Summary	Application No. 08/781,188	Applicant(s) shin
	Examiner Tiep Nguyen	Group Art Unit 2515

☐ Responsive to communication(s) filed on ______.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *7-9, 11-15, and 17-20* is/are pending in the application.

Of the above, claim(s) ______ is/are withdrawn from consideration.

☒ Claim(s) *15 and 17-20* is/are allowed.

☒ Claim(s) *7-9, 11, 13, and 14* is/are rejected.

☒ Claim(s) *12* is/are objected to.

☐ Claims ______ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *08/616,291*.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- *SEE OFFICE ACTION ON THE FOLLOWING PAGES* ---

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8,11,14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kakuda'933.

The above claims are anticipated by Kakuda's figure 6 which discloses a wiring structure of an LCD device comprising:

- a substrate (10);
- a first conductor (29L) formed on the substrate as claimed;
- a first insulative layer (12) having a first via hole (28) exposing a portion of the first conductor;
- a second conductor (32L) formed on a portion of the first insulative layer as claimed;
- a second insulative layer (25) having a second via hole (28) and third via hole (28) as claimed;
- a third conductor (31) as claimed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7,9,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuda'933.

Regarding the above claims, Kakuda discloses the claimed invention except for the use of ITO for the third conductor. The use of such material for conductors in LCD devices is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use ITO for the third conductor because such material has been proven in the art as a good and reliable conductor; furthermore, its thin-film characteristics is especially beneficial for use in LCD devices where compactness and minimal overall thickness of the devices are desired.

Allowable Subject Matter

5. Claims 15, 17-20 are allowed.

6. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Tiep H. Nguyen whose telephone number is (703) 305-3496.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1615.

William L. Sikes

WILLIAM L. SIKES
SUPERVISORY PATENT EXAMINER
GROUP 2500

EXHIBIT C-3

OIPE JC10
NOV 17 1997
PATENT & TRADEMARK OFFICE

PATENT
Attorney Docket No. 4805.0110-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

61B
Jesa
12-2-97

In re Application of:)	
Woo Sup SHIN)	
Serial No.: 08/781,188)	Group Art Unit: 2515
Filed: January 10, 1997)	Examiner: T. Nguyen
For: LIQUID CRYSTAL DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME)	

RECEIVED
DEC 01 1997
GROUP 2500

Sir:

Amendment

In response to the Office Action mailed on August 1, 1997, the period for response to which extends through December 1, 1997, by reason of a petition and fee for a one-month extension of time filed concurrently herewith, please amend the application as follows:

IN THE CLAIMS

Please cancel claim 12 without prejudice or disclaimer and amend claims 7, 8, 11, and 14 as follows:

1 ~~7~~. (Amended) A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

B1

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a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

B' cont.

18. (Amended) A wiring structure comprising:

a substrate;

a first [conductor] conductive layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first [conductor] conductive layer;

a second [conductor] conductive layer formed on a portion of said first insulative layer;

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B3 cont.

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes;

<u>wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor</u>.

B3

~~11~~6. (Amended) A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said [substrate] <u>primary</u> surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

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B2 Cont.

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

8 ~~14~~. (Amended) A method of manufacturing a liquid crystal display device, comprising the steps of:

B3

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively.

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Remarks

In the Office Action, the Examiner rejected claims 8, 11, and 14 under 35 U.S.C. § 102(b) as anticipated by Kakuda et al. (U.S. Pat. 5,162,933) and rejected claims 7, 9, and 13 under 35 U.S.C. § 103(a) as unpatentable over Kakuda et al. In addition, the Examiner allowed claims 15 and 17-20 and objected to claim 12, but indicated that it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As indicated above, the Examiner allowed claims 18-20. However, claims 18 and 19 depend from rejected claim 8, and claim 20 depends from rejected claim 14. Therefore, it is unclear whether the Examiner mistakenly allowed the claims or intended to object to the claims as being allowable but depending from a rejected base claim. Applicant respectfully request clarification of the Examiner's action regarding claims 18-20.

By this Amendment, Applicant has amended claim 11 essentially to include the recitations of canceled claim 12. As amended, claim 11 recites that a wiring structure includes a third conductive layer formed on a second insulating layer and electrically connected to first and second conductive layers via first and second contact holes, wherein one of the first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor. The terminals of a thin film transistor correspond to the gate, source, and drain.

The Examiner rejected claims 8, 11, and 14 under §102(b) as anticipated by Kakuda et al. Kakuda et al. discloses that connection land 29L is formed integrally with

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one end portion of each storage capacitor line 29, and connection land 32L is connected via a wire 32W to an external connection terminal 32X formed integrally with wire 32W at one marginal position of a base plate 10 (column 5, lines 6-20). Therefore, Kakuda et al. fails to disclose or suggest connection lands 29L or 32L being connected to a terminal of a thin film transistor. Thus, claim 11 is patentably distinguishable from Kakuda et al.

Claim 8, as amended, recites a wiring structure similar to claim 11, including one of the first and second conductive layers being connected to one of a plurality of terminals of a thin film transistor. Therefore, claim 8 is patentably distinguishable from Kakuda et al. for the same reasons as claim 11.

Claim 14 has been amended to recite a method of manufacturing a liquid crystal display device, including the steps of forming a first conductive layer pattern on a substrate, the first conductive layer pattern being connected to a first terminal of a thin film transistor and forming a second conductive layer pattern on a first insulating layer, the second conductive layer pattern being connected to a second terminal of the thin film transistor. Therefore, claim 14 is also patentably distinguishable from Kakuda et al. for the same reasons as claim 11.

The Examiner also rejected claims 7, 9, and 13 under § 103 as being unpatentable over Kakuda et al. In particular, the Examiner admitted that Kakuda et al. does not disclose the use of ITO for the third conductor. The Examiner asserted, however, that the use of ITO as a conductor in an LCD device is well known in the art.

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Even if the Examiner's assertion is correct, Kakuda et al. fails to render obvious claims 7, 9, and 13. In particular, claim 7, as amended, recites that a wiring structure similar to claim 11 includes one of the first and second conductive layers being connected to one of a plurality of terminals of a thin film transistor, which Kakuda et al. fails to disclose or suggest as discussed above with respect to claim 11. Therefore claim 7 is patentably distinguishable from Kakuda et al. Claims 9 and 13 are also patentably distinguishable from Kakuda et al. by reason of their dependence from claims 8 and 11, respectively, as well as their additional recitations.

In addition, claims 18-19 and 20 are also patentably distinguishable from Kakuda et al. by reason of their dependence from claims 8 and 14, respectively, as well as their additional recitations.

Applicant respectfully submits that claims 7-9, 11, 13-15, and 17-20 are in condition for allowance. Reconsideration of the application and the allowance of the pending claims are respectfully requested.

To the extent any extension of time under 37 C.F.R. 1.136 is required to obtain entry of this response, such extension is hereby requested. If there are any fees due under 37 C.F.R. 1.16 or 1.17 which are not enclosed, including any fees required for an

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extension of time under 37 C.F.R. 1.136, please charge those fees to our Deposit Account No. 06-916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: ______________________
Andrew Chanho Sonu
Reg. No. 33,457

Dated: November 17, 1997

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EXHIBIT C-4

UNITED STATES PATENT APPLICATION FOR

LIQUID CRYSTAL DISPLAY DEVICE

AND A METHOD OF MANUFACTURING THE SAME

BY

WOO SUP SHIN

WHAT IS CLAIMED IS:

1. A pad for providing and electrical connection to a data electrode of a switching device, said pad comprising:

a portion of said data electrode; and

a layer of indium tin oxide provided on said portion of said data electrode.

2. A liquid crystal display device comprising:

a switching element having a data electrode; and

a pad including a portion of side data electrode and a layer of indium tin oxide provided on said data electrode and a layer of indium tin oxide provided on said portion of said data electrode.

3. An electrical contact comprising:

a substrate;

a conductive layer formed on said substrate;

First and second insulative layers formed on said conductive layer, said first and second insulative layers including a common hole exposing a portion of said conductive layer, a sidewall of said hole being substantially smooth; and

a layer of indium tin oxide (ITO) provided on said exposed portion of said conductive layer.

4. A liquid crystal display device comprising:

a data line; and

a pad, said pad including:

a portion of said data line, and

a layer of indium tin oxide (ITO) provided on said data line.

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5. A pad comprising:

a substrate;

a first insulative layer having a contact hole exposing a portion of said substrate;

a second insulative layer having a second contact hole aligned with said first contact hole;

a first conductive layer formed on said exposed surface of said substrate; and

a second conductive layer formed on said first conductive layer.

6. A pad in accordance with claim 5, wherein said second conductive layer includes indium tin oxide.

7. A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layer to expose part of said first conductive layer and a second contact hole is provided through

said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer.

8. A wiring structure comprising:

a substrate;

a first conductor layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of the first conductor layer;

a second conductor formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer; and

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes.

3 ~~9~~. A wiring structure in accordance with claim 2 ~~8~~, wherein said third conductive layer includes indium tin oxide.

10. A method of manufacturing an electrical contact structure comprising the steps of:

depositing a first conductive layer on a surface of substrate;

depositing a first insulative layer on said first conductive layer and said surface of substrate;

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depositing a second insulatvie layer on a portion of said insulative layer overlying said first conductive layer;

selectively removing, in a single etch step, portions of said first and second insulative layers to expose a part of said first conductive layer; and

depositing a layer of indium tin oxide on said exposed portion of said first conductive layer.

Sub B2

11. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said substrate surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes.

12. A liquid crystal display device in accordance with claim 11, wherein said first conductive layer is a gate electrode and said second conductive layer is a source

electrode.

12 ~~13~~. A liquid crystal display device in accordance with claim 6 ~~11~~, wherein said third conductive layer includes material suitable for forming a pixel electrode.

Sub B3

~~14. A method of manufacturing a liquid crystal display device, comprising the steps of:~~

~~forming a first conductive layer pattern on a substrate;~~

~~forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;~~

~~forming a second conductive layer pattern on said first insulating layer;~~

~~forming a second insulating layer overlying said substrate including said second conductive layer pattern;~~

~~selectively etching said first and second insulating layer to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and~~

~~forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and conductive layer patterns via said first and second contact holes, respectively.~~

14 ~~15~~. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including:

a gate electrode,

a gate pad, and

a source pad;

a gate insulating film on said surface of said substrate,

a portion of said gate insulating film overlying said gate electrode;

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer;

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

16. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode and a gate pad;

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forming an insulating film on said substrate including said gate electrode and said gate pad;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

selectively removing a portion of said impurity doped semiconductor layer and said semiconductor layer, except for a portion overlying said gate electrode;

forming a second conductive layer on said substrate;

pattering said second conductive layer to form a source electrode, a source pad, and a drain electrode, said source electrode connected to said source pad;

forming passivation film on the entire surface of said subsrate;

selectively etching said passivation film and said insulating film to form a first contact hole to expose said source pad, a second contact hole to expose a portion of said drain electrode, and a third contact hole to expose said gate pad;

forming a transparent conductive layer on said substrate; and patterning said transparent conductive layer to form a first transparent conductive layer pattern connected with said source pad via said first contact hole, a pixel electrode connected with said drain electrode through said secnond contact hole, and a second transparent conductive layer connected with said gate pad through said third contact hole.

|| ~~17~~. A method of manufacturing a liquid crystal display device, comprising the steps of:

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forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

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ABSTRACT OF THE DISCLOSURE

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

EXHIBIT C-5

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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

WESTERN DIVISION

LG PHILIPS LCD CO., LTD., Plaintiff v. TATUNG CO. OF AMERICA, TATUNG COMPANY and CHUNGHWA PICTURE TUBES, LTD., Defendants.	No. CV 02-6775 CBM (JTLx) **ORDER RE CLAIM CONSTRUCTION**

DOCKETED ON CM
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BY 001

The matter before the Court is claim construction regarding the side-mount patents and semiconductor patents. The claim construction hearing occurred on January 13-14, 2005, the Honorable Consuelo B. Marshall presiding.

JURISDICTION

This Court has jurisdiction pursuant to 28 U.S.C. §1331.

FACTUAL AND PROCEDURAL BACKGROUND

L.G. Philips LCD Co, Ltd. ("LPL") filed this action on August 29, 2002, alleging that Defendants Tatung Co., Tatung Co. of America, and Chunghwa Picture Tubes ("CPT") infringed on its patents. On December 20, 2002, CPT filed an Answer and Counterclaims. On August 31, 2004, this Court granted in part CPT's motion for leave to amend its Answer and Counterclaims and to Join

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LGE as a party. On October 12, 2004, this Court denied LPL's motion to stay further proceedings pertaining to the side-mount patents and set the claim construction hearing for January 7, 2005. On its own motion, the Court continued the claim construction hearing to January 13, 2005.

LEGAL STANDARD

In interpreting an asserted claim, the Court first looks to the intrinsic evidence, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576 (Fed. Cir. 1996). However, all intrinsic evidence is not equal. First, the Court should focus on the claims themselves, both asserted and unasserted, to define the meaning and scope of the patented invention. *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1201-02 (Fed. Cir. 2002). There is a "heavy presumption" that the ordinary and accustomed meaning of a claim term, as understood by one of ordinary skill in the art, is the correct construction. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). Dictionaries, encyclopedias and treatises, which are extrinsic evidence, may be employed to "assist the court in determining the ordinary and customary meanings of claim terms." *Texas Digital*, 308 F.3d at 1202.

Second, the Court should review the specification. *Vitronics*, 90 F.3d at 1582. A review of the specification will reveal whether or not the inventor has given a term an unconventional meaning. *Id.* However, it is improper to read a limitation into a claim from the specification. *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182 (Fed. Cir. 1998). The inventor may act as his or her own lexicographer and use terms in a manner other than their ordinary meaning, so long as any such specific definition is clearly stated in the patent specification or prosecution history. *Mycogen Plant Science Inc. v. Monsanto Co.*, 243 F.3d 1316, 1327 (Fed. Cir. 2001). Therefore, for claim construction purposes, the specification is "the single best guide to the meaning of a disputed term."

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Vitronics, 90 F.3d at 1582.

Third, the Court may consider the prosecution history of the patent. The prosecution history is significant because it reveals "the course of dealing with the Patent Office, which may show a particular meaning attached to the terms, or a position taken by an applicant" to secure the patent. *Markman*, 52 F.3d at 991. As such, the prosecution history may be reviewed to assess whether a patentee "relinquished [a] potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a [prior art] reference." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999), *cert. denied*, 529 U.S. 1066 (2000). However, for subject matter to be held relinquished, a court must find that the patentee disclaimed the subject matter with "reasonable clarity and deliberateness." *Northern Telecom Ltd. v. Samsung Electronics Co., Ltd.*, 215 F.3d 1281, 1294 (Fed. Cir. 2000).

Finally, if and only if a claim remains "genuinely ambiguous" despite the full consideration of the intrinsic evidence, then a court may look toward extrinsic evidence to interpret the claim term itself. *Bell & Howard Document Mgmt. Prods. Co. v. Altek Sys.*, 132 F.3d 701, 706 (Fed. Cir. 1997). The need for such a departure from the intrinsic evidence "rarely, if ever, occurs." *Vitronics*, 90 F.3d at 1585.

ANALYSIS

A. Side-Mounting Patents

The side-mounting patents consist of U.S. Patents Nos. 6,373,537 ('537 patent), 6,00,457 ('457 patent), 6,020,942 ('942 patent), and 5,926,237 ('237 patent).

1. Whether the Side-Mounting Patents Are Limited to Portable Computers

The definition of the terms "liquid crystal display," "liquid crystal panel," "housing" and "outer casing" are disputed because CPT limits them to "portable

computers" whereas LPL does not so limit them. The '537 and '237 patents contain claims directed to both an LCD device and to a portable computer, whereas the '457 patent contains claims directed only to the LCD device and the '942 patent contains claims directed only to a portable computer. Since the Court must look first to the claims, the Court finds that claims that recite a "portable computer" are limited to portable computers, but claims that do not recite a "portable computer" are not so limited. The background of the invention also indicates that the portable computer is *an example* of a device that uses an LCD. *See, e.g.,* 1:50-51 ("[t]he liquid crystal display is usually combined with, *for example,* a notebook computer for use as an output screen"; 1:59-61 ("a liquid crystal display is attached to a device *such as a notebook computer*") . With respect to the terms "housing" and "outer casing," the Court notes that independent claims, such as Claim 37 of the '457 patent, which contain the term "housing" do not contain the words "portable computer," whereas dependent claim 40 of the '457 patent states "the housing includes a portable computer." This indicates that the definition of the terms should not be limited to a portable computer.

Defendants look at the specification, rather than first looking to claims, in arguing that the invention described in the specification is directed to an improvement for a portable computer. Defendants' argument is not persuasive, as the Federal Circuit has held that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Liebel-Flarsheim Co. v. Medrad, Inc.,*358 F.3d 898, 906 (Fed. Cir. 2004); *accord Gemstar-TV Guide Int'l Inc. v. ITC,* 383 F.3d 1352, 1366 (Fed. Cir. 2004). The specification of the side-mounting patents does not contain any "clear disavowal" of products that are not portable computers. In addition, this Court rejects Defendant's argument that the

sidemounting patents should be limited to portable computers because that was the purported "object" of the invention. "The fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives." *Liebel,* 358 F.3d at 908. *See also Ex-Pass Tech, Inc. v. 3Com Corp.,* 343 F.3d 1364, 1370 (Fed. Cir. 2003) ("The Court's task is not to limit claim language to exclude particular devices because they do not serve a perceived "purpose" of the invention."). Thus, the Court adopts LPL's definitions of the terms "liquid crystal display," "liquid crystal panel", "housing" and "outer casing."

2. Whether Constructions Should Include the Word "Directly"

The word "directly" does not appear anywhere in the claim language. However, Defendants use the word "directly" in construing the terms "attachable to a housing," "fixable to a housing," "joined with," "joining together,""coupled," and "fastening part." Defendants argue that the claim language, in context, indicates that side-to-side direct connection must be present, as the specification does not show any intervening element. The Court finds Defendants' arguments unpersuasive pursuant to *Liebel,* which makes it clear that the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction. Since no such words of manifest exclusion or restriction are used here, the Court adopts LPL's definitions of "attachable to a housing" or "fixable to a housing," "joined," "joined together," "coupled," and "fastening part."

3. Whether the terms "through" and "passing through" should have different meanings

LPL proposes that the term "through" be used in its plain and ordinary way to mean "by way of," and that "passing through" means "extending into." Defendants contend that "through" means "in at one end, side or surface and out

the other" and that "passing through" means "moving past or making way in one side and out of the other side." Although the preferred embodiment shown in the drawings uses screws engaging holes to connect the components, the patent clearly contemplates other methods of attaching the components. The '457 patent specification, for example, provides that "an adhesive device, such as double-sided tape can be used instead of the second and third screw holes" and that "the rear case 500 and the second support frame 400 are jointed to each other using hooks and/or other suitable fastening devises, including adhesives." *See, e.g.,* 4:58-60, 4:63-67. Since LPL's definition of "through" covers both screws and adhesives, the Court finds that it is the better definition.

LPL contends that the phrase "passing through," in contrast to "through," is used only in reference to screws and screw holes, which extend into an object. CPT, on the other hand, argues that "passing through" and "through" have the same meaning. The doctrine of claim differentiation indicates that different words or phrases used in different claims are presumed to indicate that the claims have different meaning and scope. *Karlin Tech, Inc. v. Surgical Dynamics, Inc.,* 177 F.3d 968, 971 (Fed. Cir. 1999). Here, it appears that the inventors used the term "through" when generally referring to a fastening part but used "passing through" only when referring to a specific fastening part (i.e.. a screw). Therefore, the Court adopts LPL's definitions of "through" and "passing through."

4. Whether the terms "frame," "first frame," and "second frame" should be given their plain and ordinary meanings.

LPL defines "frame" to mean "a support structure." Defendants defines "Frame" as "an open structure or rim for encasing, holding or bordering that encloses a substantial portion of each side edge of another structure." Defendants base their argument on the theory that the meaning of the word "frame" is limited to the description in the specification. Under *Liebel,* this restrictive interpretation is inappropriate. Furthermore, Defendants define "first" and "second" frame to

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mean "inner" and "outer" frame, even though the inventors did not use those terms. The use of "first" and "second" follow the "common patent-law convention to distinguish between repeated instances of element or limitation." *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). For example, Claim 31 of the '942 patent claims "[t]he portable computer according to claim 13 wherein the fastening part includes first and second screws passing through first and second holes at a same side edge of at lease one of the first and second frames." 8:25-28. Here, the words "first" and "second" are consistently used to distinguish repeated instances of element or limitation. Therefore, the Court gives "frame," "first frame" and "second frame" their ordinary meanings, as set forth by LPL.

5. Whether "liquid crystal display model" is a typographical error

The parties agree on the construction of the claim term "liquid crystal display module." However in one claim, Claim 7 of the '537 patent, the term appears as "liquid crystal display model." Given the context, this is clearly a typographical error. Other parts of Claim 7 refer to the "liquid crystal display module." The Court therefore construes "liquid crystal display model" as "liquid crsytal display module."

6. Whether Definitions are Needed for "Portable Computer," "Side", "Forming" and "Cover"

Defendants propose cumbersome definitions for the terms "portable computer," "side", "forming" and "cover." The Court finds that these definitions create unnecessary confusion and adopts LPL's constructions, which give the terms their plain and ordinary meaning.

B. Construction of the '737 Semiconductor Patent

1. "Source Electrode," "Drain Electrode," and "Gate Electrode"

While LPL construes the electrode to include the line and the pad, Defendants limits the electrode to a single TFT and construes the electrodes as

distinct from the lines and the pads. The seventh step of claim 1 of the '737 patent calls for "exposing a part of each of said source electrode, drain electrode and gate electrode." LPL persuasively argues that electrodes are exposed at the pad region for electrical connection, as exposing a gate pad allows electrical control of all TFT gate contacts along the row. One of ordinarily skill would not control each TFT gate/source independently, especially since creating a hole at each TFT to expose the gate electrode would destroy the TFT. Furthermore, the specification of the '737 patent describes a step in which "gate electrode 2 extending along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate." 3:25-28. This indicates that a structure separate from the TFT is part of the "gate electrode." In addition, the claims in the application for the '449 patent include phrases such as "said pad comprising: a portion of said data electrode" and "a pad including a portion of [said] data electrode." Finally, U.S. Patent 4,705,358 ('358 patent), which also pertains to the same technology as the '737 patent, names the same inventor as the '737 patent, and was filed in the U.S. on the same day as the '737 patent, illustrates a gate electrode from above (i.e. a "bird's-eye-view") and demonstrates that the "gate electrode" may include the gate line. The Court therefore finds that the electrodes may include the lines and pads. Furthermore, the Court is not persuaded by that portion of Defendant's construction which specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Continuously Depositing"

LPL construes the term "continuously depositing" as "[t]he formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films." Defendants offer a modified construction of this term

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as meaning that "the deposition of the specified films occurs without any non-deposition related steps between or during the deposition of each constituted film." While LPL's definition requires the films to be only spatially continuous, Defendants' definition requires continuity in space, time and sequence. The '737 patent shows "continuously deposited" films as being *spatially* continuous, but it does not show, mention or require the deposition to be performed without an interruption in time or sequence. Moreover, the plain meaning of "continuous" is "uninterrupted extension in space, time *or* sequence." The Court therefore adopts LPL's construction of "continuously depositing."

3. "Oxidizing atmosphere"

Claim 1 of the '737 patent requires "continuously depositing [the films] . . . without exposing them to an oxidizing atmosphere." LPL construes "an oxidizing atmosphere" as "an atmosphere that would create *substantial oxidation* on a film." The Court finds that the word "substantial" in this construction is vague and ambiguous. Defendants initially construed this phrase to mean that the films are not permitted to be exposed to *"an oxide,"* although they acknowledged that a *de minimus* amount of oxidation is not an "oxidation atmosphere." Defendants subsequently modified their construction to be "an atmosphere that would create a *detectable amount* of oxidation on a film." As "detectable" is more precise than "substantial," the Court adopts Defendants' modified construction of this term.

4. "Island region"/ "island region on said gate electrode"

At the time the patent application was filed, there were at least two well-known constructs for the semiconductor region in a TFT. In one design, separate islands of semiconductor are created above each TFT's gate electrode. In the other design, a single, unitary semiconductor region extends over all of the TFTs in one large "continent." While LPL construes the term "island region" as used in the '737 patent to include both designs, Defendants' construction limits this term to the first design (i.e. a region located over the gate electrode *of a single TFT*).

Defendants also require the island to have been "etched around its entire perimeter."

Defendants' argument is persuasive, as claim 1 recites a process for producing *"a* thin-film transistor." 4:26. *See also* 1:5, 13, 29, 57, 65, 67; 2:9; 3:34-35. Furthermore, in discussing FIG. 3b, the specification provides that "said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are *left as an island region in the area where a thin-film transistor is to be formed.*" 3:34-35. This statement indicates that the "island region" is limited to the area of a single TFT and does not include multiple TFTs. Thus, the Court finds that Defendants' construction more accurately reflects the language of the claim and the specification. Moreover, LPL's construction appears to read the term "island region" completely out of the third step, "in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left *as an island region* on said gate electrode." The Court therefore adopts Defendants' construction of the term "island region."

5. "Conducting Film Containing at Least a low-resistivity Semiconductor Film"/ "Conducting Film"/ "High-resistivity Semiconductor Film"/ "Low-Resistivity Semiconductor Film"

The '737 patent discloses two preferred embodiments. One embodiment includes four continuously deposited films: an insulating film, a high-resistivity semiconductor films, a low-resistivity semiconductor film, and a conducting film. *See* 2:17-21, Fig. 2a-2e. The other embodiment has three continuously deposited films: an insulating film, a high-resistivity semiconductor films, and a low-resistivity semiconductor film. *See* 2:24-30, Fig. 3a-3d.

Claim 1 of the '737 patent sets forth "a second step for continuously depositing . . . a gate insulating film, a high-resistivity semiconductor film and a *conducting film containing at least a low -resistivity semiconductor film.*" Claim 2, which is not at issue in this litigation, sets forth a second step wherein "said

conducting film is composed of *at least two layers consisting of a low-resistivity semiconductor films and thereon a refractory metal film or transparent conducting film*."

According to LPL, the italicized phrase in Claim 1 above means that the conducting film may consist only of a low-resistivity semiconductor film. CPT, on the other hand, construes this phrase as requiring a conducting film with adjoining layer of low resistivity semiconductor and possibly other adjoining layers. CPT relies on a sentence in the specification discussing Fig. 3a-3d, which states that, "[i]n this example, *no conducting film is formed on low-resistivity amorphous silicon film 20*, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2."[1] While this sentence does suggest that the conducting film is distinct from the low-resistivity semiconductor film, CPT's interpretation would narrow the scope of Claim 1 to exclude the second embodiment. A claim construction that excludes a preferred embodiment is "rarely, if ever, correct." *Dow Chemical Co. v. Sumitomo Chemical Co.*, 257 F.3d 1364, 1378 (Fed. Cir. 2001). Furthermore, the fact that the conducting film is specifically described as having *two layers* in claim 2 but not in claim 1 indicates that two adjoining layers are not needed for the first claim. Thus, the Court adopts LPL's construction of the term "conducting film containing at least a low-resistivity semiconductor film."

LPL's construction of "conducting film" is consistent with this Court's determination that the conducting film can be the low -resistivity semiconductor film. LPL construes "conducting film" according to its plain meaning, namely, a thickness of electrically conductive material. Defendants' construction of conducting film, on the other hand, restricts it to film "having an electrical

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[1] LPL submits intrinsic evidence in the form of a scientific article describing ITO (indium tin oxide) as a "semiconductor." This supports LPL's position that the conducting film can be the low-resistivity semiconductor.

resistance several order of magnitude lower than a low-resistivity semiconductor film." In other words, Defendants define "conducting film" as distinct from "low-resistivity semiconductor film." The Court rejects Defendants' construction and adopts LPL's construction since it finds that the conducting film in claim 1 of the '737 patent may consist of the low-resistivity semiconductor film, as discussed above.

LPL's constructions of "high-resistivity semiconductor film" and "low-resistivity semiconductor film" distinguishes these terms based on their relative resistivity. Defendants distinguish the terms according to whether they are "doped" (i.e. intentionally mixed with impurities) or "undoped." The '737 patent makes no mention of the terms "doped" and "undoped." Furthermore, LPL presents evidence that it is improper to equate the terms high-resistivity with "undoped" and low-resistivity with "doped." The Court therefore rejects Defendants' method of distinguishing these terms. Defendants also rely solely on extrinsic evidence in defining high-resistivity semiconductor film as having a resistence "many orders of magnitude" greater than the low-resistivity film. The Court finds this language vague and unnecessary. The Court therefore adopts LPL's constructions of the terms "high-resistivity semiconductor film" and "low-resistivity semiconductor film."

6. "Mask"/ "At least a part of the Mask"/ "Said source and drain electrodes serving as at least part of the mask"

Claim 1 requires a step for selectively removing material "with said source and drain electrodes serving as at least part of the mask." The parties dispute whether an electrode covered by photoresist serves as at least part of the mask. Defendants' construction may exclude such an electrode, as it requires that the source and drain electrodes "make a *significant contribution* to defining the edges of the selectively removed region" or alternatively "*shield at least part of the surface* from the action of the removal technique." While the photoresist may be

the *outermost* layer of the mask, the electrodes are part of the mask structure, as, they, too, are resistive to the removal technique and in the pattern needed to etch exposed conductive film. LPL construes "mask" as "a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed." The Court finds that this definition best explains the mask, as well as how the electrodes serve as "at least a part of the mask." The Court does not need to construe "said source and drain electrodes serving as at least part of the mask," since this phrase simply combines the terms "source electrode," "drain electrode" and "at least a part of the mask."

7. "Thin Film Transistor"

LPL's and Defendants' construction of "thin film transistor" ("TFT") are very similar. They differ in one respect: LPL specifies that TFTs are not constructed in a single crystal silicon wafer. Since the single wafer is mentioned in the intrinsic evidence and Defendants do not deny that TFTs are constructed in a single crystal silicon wafer, the Court adopts LPL's construction.

8. "A fourth step for selectively forming a source electrode and drain electrode"

LPL's construction of "a fourth step for selectively forming a source electrode and drain electrode" requires the source and drain electrodes to be "formed together." The Court finds nothing in the claim or specification that supports this interpretation. Although the formation of the source and drain electrodes is listed in one step, nothing suggests that each action within each step must be performed together. LPL's argument that the objective of the invention supports this interpretation is unpersuasive in light of *Liebel,* discussed above. However, the Court also finds Defendants' construction problematic. Defendants construe this phrase as "forming a source electrode and drain electrode in selected regions only by depositing a conducting film or other material such as Al."

Figures 1-3 and the specification do indicate that the source and drain electrode are formed in selected regions. *See* 1:15-17, 2:10-14,, 3:36-44. However, the specification does not support the second part of CPT's construction. Rather, the specification indicates that source and drain electrodes can be formed via deposition *and subsequent etching of conductive material.* The Court therefore modifies Defendant's construction and defines the phrase as "forming a source electrode and drain electrode in selected regions only," which is consistent with the Court's construction of "selectively forming" below.

9. "Contacting a part of the surface of said island region"

LPL construes "contacting a part of the surface of said island region" to mean "[f]orming an electrical connection to a part of the surface of the island region" while Defendants construe it to require "touching a part of the surface of the island region." The Court finds that Defendants' construction better reflects the plain meaning of the claim.

10. "Forming . . . on"

The first step of claim 1 is "for forming a gate electrode on an insulating substrate." LPL argues that the '737 patent uses "forming" in the sense of "providing" whereas Defendants construe "forming" as to give "form or shape to." The Court finds it awkward to define "forming" as "providing" in the phrase "selectively forming a gate electrode 2 on an insulating substrate 1," which is offered as intrinsic evidence by both parties. Defendants' construction is more meaningful in this specific context as well as in the specification and the claims as a whole. Moreover, Defendant's construction is consistent with this Court' definition of "a fourth step for *selectively forming* a source electrode and drain electrode." The Court therefore adopts Defendants' construction of "forming . . .on."

11. "Selectively etched"/ "Selectively forming"/ "Selectively removing"

Claim 1 recited a third step wherein "said high-resistivity semiconductor film and said conducting films are *selectively etched* so that they are partly left as an island region on said gate electrode." LPL defines "selectively etched" as the "removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface." Defendants object to this definition because it refers to removal of portions of a *surface*, rather than the *entire film*. While the claim does specifically refer to the etching of the high-resistivity semiconductor film and the conducting films, the Court finds nothing in the language of the claim or the specification that requires etching of the *entire* film. Furthermore, Defendants' construction, which requires etching of the high-resistivity semiconductor film, the conducting film, and the low-resistivity semiconductor film, is inconsistent with both the language of the claim and with this Court's finding that the conducting film may constitute the low-resistivity semiconductor film. The Court therefore adopts LPL's definition of "selectively etched."

In addition, Claim 1 recites a fourth step for "selectively forming a source electrode and a drain electrode," and a fifth step for "selectively removing said conducting film exposed on said island region." The Court finds no substantive difference between LPL's and Defendants' constructions of "selectively forming" and "selectively removing." However, the Court adopts Defendants' definitions of these respective terms as "forming in selected regions only" and "removing selected regions only" because they convey the meaning in the simplest language.

C. Construction of Disputed Terms of the '449 Patent

1. Gate Electrode/ Source Electrode

Defendants construe the gate/ source/ data electrodes to exclude the lines and pads. Claims 10 and 11 of the '449 patent do refer to the gate electrode, gate pad, source electrode, and source pad individually. For example, claim 10 recites that the liquid crystal display device is comprised of "a first conductive layer . . .

including: *a gate electrode, a gate pad*, and a source pad." (7:34-39). The specification, however, provides additional information that helps clarify the relationship between the electrodes and the pads. In Figures 2d and 2e, the source pad and source electrode are shown as one connected structure, although they are labeled 7 and 7A respectively. In discussing Figure 2c, the specification states that "*[s]ource electrode 7* thus forms part of a transistor region *and serves as source pad 7A* above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT." (4:1-5). In discussing Figure 2e, the specification states that "ITO pattern 6A is provided on *source pad 2A, which is part of a data electrode of the LCD*." In describing the second embodiment depicted in Figure 3, the specification provides that "source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed." Thus, while the source pads and electrodes are formed separately, they are then connected and the specification's language indicates that they are not necessarily distinct structures. The originally filed application during the prosecution of the '449 patent also supports LPL's position that the electrode should not be defined as excluding the line and pad. The first claim of the original application recites "[a] pad for providing an[] electrical connection to a data electrode of a switching device, said *pad comprising: a portion fo said data electrode* . . . ."[2] The fourth claim in the original application recites "a liquid crystal display device comprising: a data line; and a pad, *said pad including: a portion of said data line*. . . ." Likewise, the intrinsic evidence does not indicate that the gate electrode must exclude the gate pad. In fact, Figures 2a-2e do not include a separate number identifying the "gate electrode." The Court therefore rejects a construction of "electrode" that specifically excludes the line and pad.

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[2]The word "data" corresponds to "source."

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The Court also rejects Defendant's construction of these terms because it specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The intrinsic evidence does not support such a limitation. Furthermore, as discussed previously with respect to the '737 patent, the embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Gate pad"/ "Source pad"

According to LPL's construction, pads are provided near the periphery of the TFT array "to receive data from a [gate or data] driving circuit." Defendants contend that this is ambiguous because other parts of the wiring, which are not pads, may also receive data from an external driving circuit. Defendants construe the pads as an element "that is necessary in order to communicate information from an external driving circuit to a [gate or source] electrode." Defendants base this construction on a sentence in the specification which states that *"a pad wiring layer* is necessary in order to communicate information from an external driving circuit to the gate and source." (1:51-53). Since the specification refers to the *pad wiring layer* as being necessary and not the pad, the Court rejects Defendants' construction and adopts LPL's constructions of "gate pad" and "source pad."

3. "On"/ "formed on"/ "disposed on"

LPL defines "on", "formed on" and "disposed on" as "touching a top or side of." LPL contrasts these terms with "overlying," which it defines as "above" something but not necessarily touching it. This Court agrees with Defendants that the specification does not support the distinction made by LPL. For example, the specification states that a "conductive layer is formed *on* the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8." (5:6-8) (emphasis added). Conductive layer 7 and 8 do not touch the substrate (see Fig. 3), yet the specification uses the word "on." *See*

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also 2:42-44; 3:50-54; 7:49-50 (all using the word "on" to describe a situation where there is no "touching"). The Court therefore adopts Defendants' definition of "on."

4. "Contact hole is provided through . . . layer"/ "Provided through"

The phrases "contact hole is provided through" and "provided through" appear only in claims 1 and 10, always in the context of a contact hole being "provided through" one or more layers of materials. Defendants construe the claim terms to mean that these holes are "made in one side and out the opposite side" of the layers of materials. The Court finds that these phrases should be given their ordinary meaning and therefore adopts LPL's constructions.

5. "Active layer"

Defendants' construction of "active layer" limits this area to the region of the semiconductor layer that forms the channel region between the source and drain electrodes. Figures 2b-e, 3 and 5 of the specification show the active layer 4 extending only under the source 7 and drain 8. However, as LPL points out, these figures do not in any way limit the extension of active layer 4 in the dimension perpendicular to the figure, or in other areas of the substrate not depicted in the cross-section views. Since nothing in the claim or specification limits the active layer to the region of semiconductor layer between the source and drain electrodes, the Court adopts LPL's construction of this term.

6. "Common hole"

LPL construes "common hole" in accordance with its plain meaning as "[a] shared hole." Defendants construe "common hole" to mean "single hole." The court finds Defendants' construction ambiguous, since it suggests that only one hole is permitted. The Court therefore adopts LPL's construction of this term.

7. "Aligned"

LPL construed "aligned" to mean "placed in line with," which is its ordinary meaning. Defendants, on the other hand, construe "aligned" to mean

"substantially co-axial or concentric." Defendants' definition would require the holes to be one on top of the other, whereas LPL's construction would permit the holes to be placed either side-by-side or on top of each other. Although the figures in the specification show these holes to be on top of each other as described by Defendants, the plain language of the claim should not be limited by the figures in the specification. *See Dayco Products,* 258 F.3d at 1327. The Court therefore adopts LPL's construction fo this term.

8. "Said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region"

Defendants' construction of "said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region" limits the phrase to mean that "the first and second contact holes must overlap." However, none of the embodiments disclosed in the '449 patent teaches that the hole exposing the second conductive layer (i.e. the "second hold") overlaps with the hole in the first insulative layer that exposes the first conductive layer. *See, e.g.,* Fig. 3 and Fig. 5. Since a claim construction that excludes from its scope a preferred embodiment is rarely, if ever, correct, the Court adopts LPL's construction.

9. "Wiring structure"

This term "wiring structure" appears in Claims 1-5 of the '449 patent. LPL's definition characterizes the term as a "slender structure" while Defendants refer to the layer simply as a "structure." Claim 1 begins with "A wiring structure comprising: a substrate . . . ." Since the substrate is typically a large slab of glass, which is not "slender," the Court adopts Defendants' definition of this term.

IT IS SO ORDERED

DATE: May 5, 2005

CONSUELO B. MARSHALL
UNITED STATES DISTRICT JUDGE

EXHIBIT C-6

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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

LG.PHILIPS LCD CO., LTD., Plaintiff, vs. TATUNG CO. OF AMERICA, TATUNG COMPANY AND CHUNGHWA PICTURE TUBES, LTD., Defendants.	Case No. CV 02-6775 CBM (JTLx) Case No. CV 03-2866 CBM (JTLx) Case No. CV 03-2884 CBM (JTLx) Case No. CV 03-2885 CBM (JTLx) Case No. CV 03-2886 CBM (JTLx) **SECOND REVISED JOINT CLAIM CONSTRUCTION STATEMENT** DATE: April 5, 2004 TIME: 3:00 p.m. PLACE: Courtroom of the Honorable Consuelo B. Marshall
LG.PHILIPS LCD CO., LTD., Plaintiff, vs. JEAN COMPANY, LTD., Defendant.	

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LG.PHILIPS LCD CO., LTD., Plaintiff, vs. LITE-ON TECHNOLOGY CORP. and LITE-ON TECHNOLOGY INTERNATIONAL INC., Defendants.	
LG.PHILIPS LCD CO., LTD., Plaintiff, vs. TPV TECHNOLOGY, LTD, and ENVISION PERIPHERALS, INC., Defendants.	
LG.PHILIPS LCD CO., LTD., Plaintiff, vs. VIEWSONIC CORPORATION, Defendant.	

Pursuant to the Court's October 1, 2003 Order regarding Claim Construction Briefing, LG.Philips LCD Co., Ltd. ("LPL"), Tatung Co. of America and Tatung Company (collectively "Tatung"), Chunghwa Picture Tubes, Ltd. ("CPT"), Jean Company, Ltd. ("Jean Co."), Lite-On Technology Corporation and Lite-On Technology International Incorporated (collectively "Lite-On"), TPV Technology, Ltd. ("TPV"), Envision Peripherals, Inc. ("Envision") and Viewsonic Corporation ("Viewsonic") submit this Second Revised Joint Claim Construction Statement consisting of Exhibits A-F.

Exhibit A is a list of claim terms for which the parties agree on a construction concerning U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237. Exhibit A is submitted on behalf of all of the parties.

Exhibit B is a list of disputed terms from U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237, along with the parties' respective constructions and support for those constructions. Exhibit B is submitted on behalf of all of the parties.

Exhibit C is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 4,624,737. Exhibit C is submitted on behalf of all of the parties.

Exhibit D is a list of disputed terms from U.S. Patent No. 4,624,737, along with the parties' respective constructions and support for those constructions. Exhibit D is submitted on behalf of all of the parties.

Exhibit E is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 5,825,449. Exhibit E is submitted on behalf of all of the parties.

Exhibit F is a list of disputed terms from U.S. Patent No. 5,825,449, along with the parties' respective constructions and support for those constructions. Exhibit F is submitted on behalf of all of the parties.

Exhibits A-F filed herewith will supercede Exhibits A-F of the Revised Joint Claim Construction Statement, filed on September 17, 2003 ("First Revised JCC"). In addition, all supporting exhibits filed by the parties in support of their respective positions are incorporated herein.

Defendants' submission of these proposed claim constructions and corresponding support should not be construed as an admission by any defendant that any of the claims are infringed, valid or enforceable. Defendants' submissions relate to those patents asserted against them in the various Complaints. Furthermore, defendants' submission of these proposed claim constructions do not

affect or waive any arguments regarding the invalidity of the patents-in-suit. The parties preserve the right to amend and/or supplement the terms and/or constructions in the attached claim charts as claim construction discovery continues and as the parties continue

to meet and confer to reduce the number of claims asserted and to reduce the number of terms for the Court to construe.

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JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT C

U.S. Patent No. 4,624,737

CLAIM TERMS	AGREED CONSTRUCTION
"surface passivation film"	A thickness of material that provides protection such as electrical stability and chemical isolation.
"insulating substrate"	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.
"on said gate electrode and substrate"	Above and supported by or in contact with the gate electrode and the insulating substrate.
"them"	The gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film.

EXHIBIT D

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D
U.S. Patent No. 4,624,737

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
thin-film transistor	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	Intrinsic Evidence: '737 Patent at col. 1, lines 6-29, 56-58, 61-68; col. 2, lines 1-2, 8-68; col. 3, lines 1-62; col. 4, lines 1-23; Figs. 1a-3d; and claims 1-4. (LPL Exh. 1). '737 patent discloses various techniques for fabricating thin films, such as chemical vapor deposition (CVD) (e.g., 2:24-33), sputtering (2:33-36), molecular beam deposition (4:19-20), ion beam deposition (4:19-20). "Any suitable means of applying the	A semiconductor device in which the current flow between source electrode and drain electrode is controlled by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate.	Intrinsic Evidence: '737 Patent, col. 1 lines 6-14; col. 2 line 61 – col. 2 line 2; col. 2 lines 8-10; col. 3 lines 22-24. Extrinsic Evidence: "Thin film technology" for circuits and systems is defined as "a technology in which a thin film (a few hundred to a few thousand angstroms in thickness) is applied by vacuum deposition to an insulating substrate." *IEEE Standard Extrinsic Evidence of Electrical and Electronic Terms* 939 (3rd ed. 1984)

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		various films throughout this procedure in the vacuum may be employed such as, for example, evaporation, sputtering, and the like." USPN 4,331,758 to Luo issued May 25, 1982, col. 4, lines 11-14 (LPL Exh. 2). "A thin-film transistor (TFT) is an insulated grid field effect transistor. It is similar to a MOS transistor (metal-oxide semiconductor) with the difference that it is produced on an amorphous substrate and *not on a*		("*1984 IEEE*"), Exh. 1. "A thin-film transistor, TFT, fabricated by evaporation of all components on to an insulating substrate has been developed" Paul K. Weimer, *The TFT – A New Thin-Film Transistor* in *49 Proceedings of the IRE* 1462-64 (1962), Exh. 2.

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D
U.S. Patent No. 4,624,737

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		monocrystalline silicon wafer. As they are not limited by the size of the crystalline substrate, TFT circuits can have very large dimensions. The TFT on an insulating substrate has been investigated in three different ways. . . ." USPN 4,426,407 to Morin et al. issued Jan. 17, 1984, col. 1, lines 13-22 (emphasis added) (LPL Exh. 3). <u>Extrinsic Evidence:</u> *The Penguin Dictionary of Electronics* 569 (3rd. ed. 1998) ("*1998 Penguin*") ("*thin-film transistor* (TFT) A		

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		MOSFET that is fabricated using thin-film techniques on an insulating substrate rather than on a semiconductor chip.") (LPL Exh. 4); *id.* at 205-207 ("*field-effect transistor* (FET) . . . It is a three terminal semiconductor device in which the current flow through one pair of terminals, the *source* and the *drain*, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by the voltage applied at the third terminal, the *gate*. . . ."); *id.* at 70		

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		("*chip* . . . A small piece of single crystal of semiconductor material containing either a single component or device or an integrated circuit."). *See also The Penguin Dictionary of Electronics*, 71, 186-192, 583 (2nd. ed. 1988) ("*1988 Penguin*") (LPL Exh. 5).		
gate electrode	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.	Intrinsic Evidence: "FIG. 2a shows in a sectional view the initial step for selectively forming a gate electrode 2 on an insulating substrate 1 .	A conductive element of a single thin-film transistor that controls the current between source and drain by a voltage applied to its terminal. The gate	Intrinsic Evidence: "Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		. . . Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode 2." '737 Patent at col. 2, lines 7-16. "FIG. 3a illustrates a step in which gate electrode 2 extending along one line and gate electrodes 2' on another line are formed on a transparent substrate 1 such as a glass substrate." '737 Patent at col. 3, lines 22-29.	electrode is distinct from the gate line and the gate pad associated with the gate electrode.	used as said gate electrode 2." '737 Patent, col. 2 lines 14-16. "FIG. 3a illustrates a step in which gate electrode 2 extending along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate." '737 Patent, col. 3 lines 26-28. *See also* Figs. 1-3; Col. 1 lines 15-17; <u>Extrinsic Evidence</u>: "Gate" is defined as a structural element of a TFT that "controls the current between

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		See also Figs. 1-3; and claim 1.		source and drain by a voltage applied to its terminal." *1984 IEEE* 384, Exh. 1. U.S. Patent No. 4,331,758 to Luo, Figures 8 and 8A, col. 7 line 17 to col. 8 line 9, Exh. 15. "Gate" is defined as "[a]n electrode or electrodes in a field-effect transistor." *See The Penguin Dictionary of Electronics*, 237 (2nd. ed. 1988) ("*1988 Penguin*"), Exh. 18.
continuously depositing	The formation of the gate insulating film, the high-resistivity	<u>Intrinsic Evidence:</u> "[A]s shown in FIG. 1b, a gate insulating	Successively depositing each constituent film on top	<u>Intrinsic Evidence</u>: "[A] gate insulating film 3, a high-

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	semiconductor film and conducting film without intervening films.	film 3 (such as silicon nitride film) and an amorphous silicon film 4 are continuously deposited. . . ." '737 Patent at col. 1, lines 17-21. "In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode	of the underlying film or structure without interruption and without performing any processing steps between the deposition of each constituent film.	resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming [films 3, 4 and 20] in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming [films 3, 4, and 20] in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film 30		the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film 30 can be also deposited continuously without exposure to the atmosphere." '737 Patent, col. 2 lines 17-36. *See also* '737 Patent Col. 1 lines 17-21, 32-54; col. 3 lines 28-35, 53-62; col. 4 lines 1-13; Abstract. <u>Extrinsic Evidence:</u>

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		can be also deposited continuously without exposure to the atmosphere." '737 Patent at col 2, lines 17-37. *See also* '737 Patent at col. 3, lines 28-35, 54-62; col. 4, lines 1-13; Abstract; Figs. 2b and 3b; and claims 1 and 2. <u>Extrinsic Evidence:</u> *The American Heritage College Dictionary* 1215 (2d College Ed. 1985) ("*1985 American Heritage Dictionary*") (defining "successive" as "[f]ollowing in an uninterrupted order or sequence.") (LPL Exh. 6); *id*. at 317 (defining		"Continuous" is defined as "marked by uninterrupted extension in space, time, or sequence." *1981 Webster's* 243-44, Exh. 3. "Continuous" is defined as "extending or prolonged without interruption or cessation; unceasing," *The American Heritage Dictionary* 317 (2d College Ed. 1985), Exh. 16. W.E. Spear & P.G. LeComber., *Fundamental and Applied Work on Glow Discharge Material*, in *The*

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		"continuous" as "extending or prolonged without interruption or cessation; unceasing"). *The American Heritage College Dictionary* 301 (3d College Ed. 1997) (defining "continuous" as "uninterrupted in time, sequence, substance, or extent") (LPL Exh. 7). *1981 Webster's* 243-44 (defining "[c]ontinuous" as "marked by uninterrupted extension in space, time, or sequence.")		*Physics of Hydrogenated Amorphous Silicon I, Chapter 3* 64-68 (J.D. Joannopoulos and G. Lucovsky eds., Springer-Verlag 1984) ("*1984 Spear*") (describing vacuum deposition systems), Exh. 4. P.G. LeComber & W.E. Spear, *The Development of the a-Si:H Field Effect Transistor and its Possible Applications*, in *21D Semiconductors and Semimetals* 89-95 (1984) ("*1984 LeComber*") (describing single and

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		(Defendant's Exh. 3.)		multi-chamber deposition systems). Exh. 5. T. Kodama et al., *A Self-Alignment Process for Amorphous Silicon Thin Film Transistors*, 3-7 IEEE Electron Device Letters 187-89 (Jul. 1982) ("*1982 Kodama*") (describing a continuous deposition process). Exh. 6. Japanese patent publication JP 56-135968 to Osada et al. published October 23, 1981, Figs. 1, 2; Cols. 7-31 (describing continuous deposition

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				of layers). Exh. 7. U.S. Patent No. 4,331,758 to Luo, Col. 1, Lines 9-54, Exh. 15.
gate insulating film	A thickness of material (such as SiNx) that has high electrical resistance and insulates the transistor gate from at least the transistor semiconductor.	<u>Intrinsic Evidence:</u> "Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film 3 from a mixed gas of SiH_4 and NH_3,. . . ." '737 Patent at col. 2, lines 24-26. "[A] multi-layer film . . . can be used as said gate insulating film 3." '737 Patent at col. 2, lines 36-38. *See also* '737 Patent at	A thickness of material (such as SiNx) that has high electrical resistance and insulates the gate electrode from the transistor semiconductor.	<u>Intrinsic Evidence</u>: '737 Patent, Figs. 1-3; Col. 1 lines 17-21; col. 2 lines 17-32, 36-38; col. 3 lines 28-35. <u>Extrinsic Evidence</u>: "Film" is defined as "a thin covering or coating" and "an exceedingly thin layer." *1981 Webster's* 425, Exh. 3. "Gate" is defined as a structural element of a TFT that "controls the current between source and drain by a

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		1:12-21, 2:18-38, 3:28-35; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d; and claim 1. <u>Extrinsic Evidence:</u> *1988 Penguin* at 194 (defining "film" as a "coating with a minimal thickness dimension.") (LPL Exh. 5). *1985 American Heritage Dictionary* at 719 (defining "layer" as a "thickness, coating, or stratum spread out or covering a surface.") (LPL Ex. 6).		voltage applied to its terminal." *1984 IEEE* 384, Exh. 1. "Insulating material" is defined as "a substance or body, the conductivity or which is zero or, in practice, very small." *1984 IEEE* 447, Exh. 1. "Layer" is defined as a "thickness, coating, or stratum spread out or covering a surface." *1985 American Heritage Dictionary* 719, LPL Exh. 6.
high-resistivity semiconductor film	A thickness of semiconductor	<u>Intrinsic Evidence:</u> "Such successive	A thickness of semiconductor with no	<u>Intrinsic Evidence:</u> "Such successive

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	material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film (later recited in the claim).	deposition can be accomplished, for instance, by . . . forming a high-resistivity a-Si:H film 4 by using SiH_4 and forming a n^+ a-Si:H film 20 from a mixed gas of PH3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus." '737 patent at col. 2, lines 23-29. "In place of said high-resistivity amorphous silicon film 4, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using,	intentionally added impurities to increase its conductivity, resulting in an electrical resistance many orders of magnitude higher than a low-resistivity semiconductor film.	deposition can be accomplished, for instance, by … forming a high-resistivity a-Si:H film 4 by using SiH_4 … in the same evacuated chamber in a plasma CVD apparatus." '737 Patent, col. 2 lines 23-29. "In place of said high-resistivity amorphous silicon film 4, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF_4, or a microcrystalline amorphous silicon

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		for instance, SiF4, or a microcrystalline amorphous silicon film." '737 patent at col. 2, lines 38-43. *See also* '737 Patent at col. 1, lines 8-29, 32-46, col. 2, lines 17-32, 38-43, 54-60; col. 3, lines 7-10, 16-21, 28-41, 48-62; col. 4, lines 1-23; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d; and claims 1 and 2. <u>Extrinsic Evidence:</u> *1988 Penguin* at 131 (defining "doping level" as a "[t]he amount of doping necessary to achieve the desired		film." '737 Patent, col. 2 lines 38-43. *See also* '737 Patent, Figs. 1-3; col. 1 lines 8-11, 17-32; col. 2 lines 17-32; col. 3 lines 28-35. <u>Extrinsic Evidence</u>: Shyh Wang, *Solid State Electronics* 129, 155 (McGraw Hill 1966) ("*1966 Wang*") (describing relative properties of conductors, semiconductors and insulators), Exh. 8 P.G. LeComber, *Doping and the Density of States of Amorphous Silicon*, in

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		characteristic in a semiconductor. Low doping levels . . . give a high-resistivity material; high doping levels . . . give a low-resistivity material.") (LPL Exh. 5). *Id.* at 194 (defining "film" as a "coating with a minimal thickness dimension.")		*Fundamental Physics of Amorphous Semiconductors* 46-55 (F. Yonezawa ed., Springer-Verlag 1981) ("*1981 LeComber*") (comparing doped and undoped semiconductors), Exh. 9. *1984 Spear* 91-97 (comparing doped and undoped semiconductors), Exh. 4. *See also 1984 LeComber* 89-95, Exh. 5; K.D. MacKenzie et al., *The Characteristics and Properties of Optimised Amorphous*

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				Silicon Field Effect Transistors, in *A31 Applied Physics A, Solids and Surfaces* 87-88 (1983) ("*1983 MacKenzie*"). Exh. 10. "Layer" is defined as a "thickness, coating, or stratum spread out or covering a surface." *1985 American Heritage Dictionary* 719, LPL Exh. 6.
conducting film	A thickness of electrically conductive material.	<u>Intrinsic Evidence:</u> Claim 1 of the '737 patent, which recites "a conducting film containing at least a low-resistivity semiconductor film." Claim 2 of the '737	A thickness which includes a material consisting of an elemental metal, metal alloy, or film of optically transparent material, and having an electrical resistance several orders of	<u>Intrinsic Evidence</u>: "[A] conducting film 30 made of a metal or other material..." '737 Patent, Col. 2 lines 17-23. "Further, when a sputtering or

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		patent, which recites "said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film." "In this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2." '737 patent at col. 3, lines 48-52.	magnitude lower than a low-resistivity semiconductor film.	metalizing chamber is additionally provided, conducting film 30 can be also deposited continuously without exposure to the atmosphere." '737 Patent, col. 2 lines 32-36. "As said conducting film 30, it is desirable to use a stable conducting film such as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like. Use of a transparent conducting film has the advantage

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		"In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 . . . ." '737 patent at col. 2, lines 17-23. "As said conducting film 30, it is desirable to use a stable conducting film such		that the process is simplified when the thin-film transistor of this invention is applied to an active matrix liquid crystal display." '737 Patent, col. 2 lines 46-53. "The same materials as used for conducting film 30 and other materials such as Al can be used for said drain and source electrode members 15, 16." '737 Patent, col. 3 lines 4-7. "In this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a

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		as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like." '737 patent at col. 2, lines 46-50. *See also* '737 Patent at col. 1, lines 25-29, 32-51, col. 2, lines 10-36, 43-68; col. 3, lines 1-10, 28-35, 48-62; col. 4, lines 1-23; Abstract; Figs. 2b-2e and 3b-3d. "Deposition of a metallic grid coating 24, e.g. of highly doped silicon or aluminum (by CVD-plasma) on the entire		conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2." '737 Patent, col. 3 lines 48-52. "The same is true with the interface of low-resistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity amorphous silicon film 20 or conducting film 30 and drain and source electrodes 15, 16 can be cleaned ..." '737 Patent, col. 3 line 57 – col. 4 line 2.

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		surface of the sample(g)." USPN 4,426,407 to Morin et al. issued Jan. 17, 1984, col. 3, lines 50-52 (LPL Exh. 3). ". . . wherein the conductive coating is of highly doped silicon and is obtained by reactive gaseous phase plasma." *Id.* at claims 5. *See also id.* at claims 1, 3, and 4. <u>Extrinsic Evidence:</u> *1985 American Heritage Dictionary* at 307 (defining "conduct[ing]" as "serv[ing] as a medium or channel for conveying") (LPL Ex.		*See also* '737 Patent, Figs. 1-3; col. 2 lines 54-60. <u>Extrinsic Evidence:</u> "Electrically conductive materials that can be prepared by CVD comprise elemental metals, metal alloys, superconductive compounds, and films of optically transparent conductors." *Thin Film Processes* 315-317 (J.L. Vossen & W. Kern eds., Academic Press 1978, Exh. 11. *See also 1966 Wang*

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		6). *1988 Penguin* at 194 (defining "film" as a "coating with a minimal thickness dimension.") (LPL Exh. 5). *CRC Handbook of Chemistry and Physics* 12-96 (75th ed., 1994-1995) (discussing the resistivity of semiconducting minerals) (LPL Exh. 9). *Thin Film Processes* 316-317 (J.L. Vossen & W. Kern eds., Academic Press 1978, (noting that "[t]hin films of optically		129, 155, Exh. 8; *1984 Spear* 91-97, Exh. 4. *See also* support cited by LPL for the term "conducting film".

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		transparent and electrically conductive materials", including SnO_2, are "usually classified" as semiconductors) (Defendants' Exh. 11).		
low-resistivity semiconductor film	A thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon, which contains phosphorous or other impurities to enhance the conductivity of the	Intrinsic Evidence: "In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1	A thickness of semiconductor having intentionally added impurities to increase its conductivity, resulting in an electrical resistance many orders of magnitude lower than a high-resistivity semiconductor film.	Intrinsic Evidence: "[A] low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 … are successively formed … Such successive deposition can be accomplished, for instance, by … forming a n+ a-Si:H film 20 from a mixed gas of PH_3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus. …"

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	film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.	without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by . . . forming a n^+ a-Si:H film 20 from a mixed gas of PH_3 and SiH_4. . . ." '737 patent at col. 2, lines 17-30. "In place of said high-resistivity amorphous silicon film 4, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF4, or a microcrystalline amorphous silicon		'737 Patent, col. 2 lines 17-32. "Such alloys [a-Si:F or a-Si:H:F alloy using, for instance, SiF_4, or a microcrystalline amorphous silicon film] can be also used for said low-resistivity amorphous silicon film 20, and such film may contain other impurites beside phosphorous impurities." '737 Patent, col. 2 lines 38-45. "In this example, no conducting film is formed on low-resistivity amorphous

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		film. Such alloys can be also used for said low-resistivity amorphous silicon film 20, and such film may contain other impurities beside phosphorous impurities." '737 patent at col. 2, lines 38-50. *See also* '737 Patent at col. 1, lines 25-29, 32-51; col. 2, lines 17-45, 54-68; col. 3, lines 1-10, 28-41, 48-62; col. 5, lines 1-23; Abstract; Figs. 1d; 2b-2e, and 3b-3d; and claims 1 and 2. <u>Extrinsic Evidence:</u> *1988 Penguin* at 131		silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2." '737 Patent, col. 3 lines 48-52. "The same is true with the interface of low-resistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity amorphous silicon film 20 or conducting film 30 and drain and source electrodes 15, 16 can be cleaned ..." '737 Patent, col. 3 line 57 –

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		(defining "doping level" as a "[t]he amount of doping necessary to achieve the desired characteristic in a semiconductor. Low doping levels . . . give a high-resistivity material; high doping levels . . . give a low-resistivity material.") (LPL Exh. 5). *Id.* at 194 (defining "film" as a "coating with a minimal thickness dimension.").		col. 4 line 2. *See also* '737 Patent, Figs. 1-3; Col. 1 lines 8-11, 17-32; col. 2 lines 32-36, 46-60; col. 3 lines 4-7. <u>Extrinsic Evidence</u>: *1984 Spear* 91-97. Exh. 4; *1984 LeComber* 89-95, Exh. 5; *1966 Wang* 129, 155, Exh. 8; *1981 LeComber* 46-55, Exh. 9; *1983 MacKenzie* 87-88. Exh. 10. "Layer" is defined as a "thickness, coating, or stratum spread out or covering a surface." *1985 American Heritage Dictionary*

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				719, LPL Exh. 6.
conducting film containing at least a low-resistivity semiconductor film	The conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films.	Intrinsic Evidence: Claim 2 of the '737 patent, which recites "said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film." *Compare* '737 patent at col. 3, lines 40-41("exposed portion of low-resisitivity amorphous silicon film 20 is removed"), Figs. 2d and 3c *with* Claim 1 ("a fifth step for selectively removing said	A conducting film with an adjoining thin layer of low-resistivity semiconductor and possibly other adjoining layers.	Intrinsic Evidence: "[A] low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed ...". '737 Patent, col. 2 lines 17-23. "In this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown

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		conducting film exposed on said island region"). Claim 1 ("a third step in which said high resistivity semiconductor film and said conducting film are selectively etched . . .") (note no separate mention is made of low resistivity semiconductor film). *See also* '737 patent at col. 1, lines 18-36, 43-57; col. 3, lines 28-41, 48-62; col. 4, lines 1-12; Figs 2b-2e, 3b-3d; claim 1. ". . . wherein the		in FIG. 2." '737 Patent, col. 3 lines 48-52. "The same is true with the interface of low-resistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity amorphous silicon film 20 or conducting film 30 and drain and source electrodes 15, 16 can be cleaned ...". '737 Patent, col. 3 line 57 – col. 4 line 2. "A gate insulating film, a high-resistivity semiconductor film, a low-resistivity

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		conductive coating is of highly doped silicon and is obtained by reactive gaseous phase plasma." USPN 4,426,407 to Morin et al. issued Jan. 17, 1984, claim 5 (LPL Exh. 3). *See also id.* col. 3, lines 50-52; claims 1, 3, and 4. <u>Extrinsic Evidence:</u> *1985 American Heritage Dictionary* at 315-316 (defining "contain" as "to have as component parts; comprise; include") (LPL Exh. 6). *1988 Penguin* at 93 (defining "conductor" as a "[a] material that		semiconductor film and if necessary a conducting film are successively deposited in lamination …". '737 Patent, Abstract *See also* '737 Patent, Figs. 2b-2e; Claim 2; Col. 2 lines 23-33, 43-54; col. 3 lines 4-7. <u>Extrinsic Evidence</u>: "Contain" is defined as "to have within," "comprise" or "include." *1981 Webster's* 242, Exh. 3 "Include" is defined as "to take in or comprise as part of a larger aggregate or principle." *1981*

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		offers a low resistance to the passage of electrical current: when a potential difference is applied across it a relatively large current flows.") (LPL Exh. 5). *Id.* at 131 (defining "doping level" as a "[t]he amount of doping necessary to achieve the desired characteristic in a semiconductor. Low doping levels . . . give a high-resistivity material; high doping levels . . . give a low-resistivity material.").		*Webster's* 576, Exh. 3. "Conducting material" is defined as "a conducting medium in which the conduction is by electrons, and whose temperature coefficient of resistivity is, except for certain alloys, nonnegative at all temperatures below the melting point." *1984 IEEE* 175, Exh. 1. "Semiconductor" is defined as "an electronic conductor with resistivity in the range between metals and insulators, in which the electric-

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				charge-carrier concentration increases with increasing temperature over some temperature range". *1984 IEEE* 815, Exh. 1. *See also 1983 MacKenzie* 87-88. Exh. 10; Japanese patent publication JP 58-190061 to Aoki et al. published November 5, 1983, Figs 4, 5; Cols. 7-9. Exh. 12.. "Layer" is defined as a "thickness, coating, or stratum spread out or covering a surface." *1985 American Heritage Dictionary*

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				719, LPL Exh. 6.
oxidizing atmosphere	An atmosphere that would create substantial oxidation on a film.	Intrinsic Evidence: "In the conventional process shown in FIGS. 1a to 1d, since the masking step precedes the deposition of n+ amorphous films 25, 26, natural oxide is produced on the exposed surface of amorphous silicon film 4. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate	An atmosphere that would create an oxide on a film.	*See support for claim term "without exposing them to an oxidizing atmosphere" below.*

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to exhibit its desired characteristics." '737 patent at col. 1, lines 32-44. "As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film 4 and low-		

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		resistivity amorphous silicon film 20, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity amorphous silicon film 20 or conducting film 30 and drain and source electrodes 15, 16 can be cleaned without damaging the high-resistivity amorphous silicon film, a good contact can be obtained without sacrificing the inherent properties of		

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		thin-film transistor." '737 patent at col. 3, line 53 – col. 4, line 2. *See also* '737 Patent at col. 1, lines 21-51; col. 2 lines 17-53; col. 3, lines 28-35, 53-62; col. 4, lines 1-23; Abstract; Figs 2b-2e, 3b-3d; and claims 1 and 2.		
without exposing them to an oxidizing atmosphere	This phrase is a combination of previously defined or agreed constructions of "them" and "oxidizing atmosphere", namely, the gate insulating film, the high-resistivity	<u>Intrinsic Evidence:</u> '737 patent at col. 1, lines 32-44, 47-53; col. 2, lines 17-36; col. 3, lines 28-35, 53-62; col. 4, lines 1-12; Figs. 2b-2e, 3b-3d; claims 1 and 2.	Without permitting the gate insulating film, high-resistivity semiconductor film, low-resistivity semiconductor film, or conducting film to come into contact with an atmosphere that would create an oxide	<u>Intrinsic Evidence</u>: "In the conventional process shown in FIGS. 1a to 1d, since the masking step precedes the deposition of n+ amorphous films 25, 26, natural oxide is produced on the

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	semiconductor film, and the conducting film containing at least a low-resistivity semiconductor film are deposited without exposure to an atmosphere that would create substantial oxidation on any of these films.		on any of these four films.	exposed surface of amorphous silicon film 4. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				exhibit its desired characteristics." '737 Patent, col. 1, lines 32-46. "[Films 3, 4, 20 and 30] are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming [films 3, 4 and 20] in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film 30 can be also deposited continuously without exposure to the atmosphere." '737 Patent, col. 2 lines 17-36. "As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film 4 and low-resistivity amorphous

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				silicon film 20, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film 20 and conducting film 30." '737 Patent, col. 3, line 53-59. "A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, …" '737 Patent,

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				Abstract. <u>Extrinsic Evidence</u>: *1984 Spear* 64-68, 91-97, Exh. 4; *1984 LeComber* 89-95, Exh. 5; *1982 Kodama* 187-89. Exh. 6; Japanese patent publication JP 56-135968 to Osada et al. published October 23, 1981, Figs. 1, 2; Cols. 7-31. Exh. 7.
selectively etched	The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.	<u>Intrinsic Evidence:</u> "Fig. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single	Have a selected portion of the substance of the conducting film, low-resistivity semiconductor film and high-resistivity semiconductor film removed using an etching technique.	<u>Intrinsic Evidence</u>: "FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, etc., can be used for this step." '737 patent at col. 2, lines 54-60. *See also* '737 Patent at col. 1, lines 14-21, 25-29, 32-35; col. 2, lines 10-16, 54-66; col. 3, lines 7-10, 28-41, 44-48; col. 4, lines 3-9; Figs. 1a-1d; 2a-2e; 3a-3e; and claim 1. USPN 4,331,758 to Luo issued May 25, 1982 (*compare* col. 7, line 39 – col. 8, line 10 (describing a wet etch) *with* col. 5, lines		masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step." '737 Patent, col. 3 lines 54-60. *See also* '737 Patent, Figs. 1-3; Col. 1 lines 17-21, 25-29; col. 2 lines 60-66; col. 3 lines 7-10, 44-48.

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		1-27 (describing the use of a non-etching technique for forming a patterned surface)) (LPL Exh. 2). <u>Extrinsic Evidence:</u> "*etching* Chemical erosions of selected portions of a surface in order to produce a desired pattern on the surface." *1988 Penguin* 170-71 (LPL Exh. 5). *Cf. id.* at 299-300 (defining "lift off"). USPN 4,404,731 to Poleshuk issued Sep. 20, 1983 (LPL Exh. 8).		
island region	A discrete portion of the high-resistivity	<u>Intrinsic Evidence:</u> "FIG. 2c illustrates the	Defendants contend that this phrase should	*See support for claim term "island region*

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	semiconductor film and conducting film that is formed by selective etching.	step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step." '737 patent at col. 2, lines 54-57. *See also* '737 Patent at col. 2, lines 54-60; col. 3, lines 28-35; Figs. 2c-2e, 3c-3d; and claim 1.	be interpreted as part of the phrase "island region on said gate electrode."	*on said gate electrode" below.*

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
island region on said gate electrode	This phrase is a combination of previously defined or agreed constructions of "island region", "on", and "gate electrode", namely, a discrete portion of the high-resistivity semiconductor film and conducting film that is formed by selective etching. The discrete portion is located above and supported by or in contact with the gate electrode.	*See* definitions of "island region" and, "gate electrode", *supra*.	Portion of the conducting film, low-resistivity semiconductor film and high-resistivity semiconductor film which has been etched around its entire perimeter into a separate isolated region located over the gate electrode of a single thin-film transistor.	Intrinsic Evidence: The '737 patent drawings show an island of material with no other surrounding material. '737 Patent, Figs. 2c, 3b. "FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step." '737 Patent, col. 2 lines 54-57. *See also* '737 Patent, col. 3 lines 28-35.

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				Extrinsic Evidence: "Island" is defined as "1: a tract of land surrounded by water and smaller than a continent 2: something resembling an island esp. in its isolated or surrounded position". *1981 Webster's* 608. Exh. 3. A.J. Snell et al., *Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels*, in 24 Applied Physics at 357, 358 (April 1981), Exh. 17.
selectively forming	Forming a pattern of	Intrinsic Evidence:	Forming in selected	Intrinsic Evidence:

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	material (for example, by depositing material and selectively etching portions of the material away).	'737 Patent at col. 1, lines 14-17, 25-29; col. 2, lines 10-36, 60-68; col. 3, lines 1-10, 24-52; col. 4, lines 3-9; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d; and claim 1.	regions only.	'737 Patent, Figs. 1-3; Col. 1 lines 15-17; col. 2 lines 10-14, 60-66; col. 3 lines 34-41; Abstract.
a fourth step for selectively forming a source electrode and drain electrode	The source electrode and drain electrode are selectively formed together.	Intrinsic Evidence: "In the next step illustrated in FIG. 3c, a transparent conducting film such as ITO film is deposited; then, drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is	Forming a source electrode and drain electrode in selected regions only by depositing a conducting film or other material such as Al.	Intrinsic Evidence: '737 Patent, Figs. 1-3; Col. 1 lines 15-17; col. 2 lines 10-14, 60-66; col. 3 lines 4-7, 36-44; Abstract.

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		removed." '737 Patent at col. 3, lines 36-41. *See also* '737 Patent at col. 1, lines 21-29, 32-51; col. 2, lines 17-68; col. 3, lines 1-14, 28-62; col. 4, lines 1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d; and claim 1.		
source electrode	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	Intrinsic Evidence: "Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15,	A conductive element of a single thin-film transistor formed over the source region from which charge carriers flow into the channel toward the drain. The source electrode is distinct from the source/data line and the source/data pad associated with the source electrode.	Intrinsic Evidence: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit." '737 Patent,

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		16 serving at least as a part of the mask. . . ." '737 Patent at col. 2, lines 60-66. "In the final step illustrated in FIG. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed (not shown)." '737 Patent at col. 3, lines 11-14. *See also* '737 Patent at col. 1, lines 21-29, 32-51; col. 2, lines 17-68; col. 3, lines 1-14, 28-62; col. 4, lines 1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d; and claim 1.		col. 1 lines 25-29. *See also* '737 Patent, Figs 1d, 2d-2e, 3c-3d; Col. 2 lines 60-66; col. 3 lines 36-41, 57-62. <u>Extrinsic Evidence</u>: "Source" is defined as a device structure which "contains the terminal from which charge carriers flow into the channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel." *1984 IEEE* 855, Exh. 1. "Source" is defined as "[t]he electrode in a

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		"[A]ll of the source electrodes 23 in any column are electrically connected together since each source electrode forms a portion of the source bus conductor. By electrically addressing any given column source bus conductor 23 and any given row gate bus conductor, a single transistor of the array can be turned on, thereby permitting current to flow from its source through the conductive channel of the semiconductive material to the corresponding drain. This then can be		field-effect transistor that supplies charge carriers (holes or electrons) to the interelectrode space." *1998 Penguin* 532, Exh. 18.

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		utilized to alter the field across an electro-optical device, such as a liquid crystal layer, thus providing an optical read-out of a bit of information." USPN 4,331,758 to Luo issued May 25, 1982 at col. 7, lines 40-58; col. 8, lines 1-10 (LPL Exh. 2). *See also id.* Figs. 8 and 8A.		
drain electrode	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the	<u>Intrinsic Evidence:</u> "Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity	A conductive element of a single thin-film transistor formed over the drain region into which charge carriers flow from the source into the channel.	<u>Intrinsic Evidence</u>: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	gate electrode.	amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask . . . ." '737 Patent at col. 2, lines 60-66. *See also* '737 Patent at col. 1, lines 21-29, 32-51; col. 2, lines 17-68; col. 3, lines 1-14, 28-62; col. 4, lines 1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d; and claim 1.		form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit." '737 Patent, col. 1 lines 25-29. *See also* '737 Patent, Figs 1d, 2d-2e, 3c-3d; Col. 2 lines 60-66; col. 3 lines 36-41, 57-62. Extrinsic Evidence: "Drain" is defined as a device structure which "contains the terminal into which charge carriers flow from the source into the channel. It has the potential which is more attractive than the source for the carriers in the

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				channel." *1984 IEEE* 276, Exh. 1. "Drain" is defined as "[t]he electrode of a field-effect transistor through which carriers leave the interelectrode space." *1998 Penguin* 152, Exh. 18.
contacting a part of the surface of said island region	Forming an electrical connection to a part of the surface of the island region.	<u>Intrinsic Evidence:</u> '737 Patent at col. 3, lines 53-62, col. 4, lines 1-2; Figs. 2d-2e; 3c-3d. <u>Extrinsic Evidence:</u> *1985 American Heritage Dictionary* at 315 (defining "contact" as a	Touching a part of the surface of the island region.	<u>Intrinsic Evidence</u>: '737 Patent, Figs. 1d, 2d-2e, 3c-3d; Col. 1 lines 25-29; col. 2 lines 60-66; col. 3 lines 36-41, 57-62. <u>Extrinsic Evidence</u>: The verb "contact" is defined as "to bring into contact with" and the noun is defined as

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		connection between two conductors that permits a flow of current") (LPL Exh. 6).		"a union or junction of surfaces" or "the junction of two electrical conductors through which a current passes." *1981 Webster's* 242, Exh. 3. The noun "contact" is defined as "the coming together or touching of two objects or surfaces." *1985 American Heritage Dictionary* at 315, LPL Exh. 6.
selectively removing	The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) or other	Intrinsic Evidence: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and	Removing selected regions only.	Intrinsic Evidence: '737 Patent, Figs. 1-3 Col. 1 lines 17-21, 25-29; col. 2 lines 60-66; col. 3 lines 7-10, 44-48.

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	techniques in order to produce a desired pattern on the surface.	selectively etched to form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit." '737 Patent, col. 1, lines 25-29. "Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5		

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		and source electrode 6." '737 Patent at col. 2, lines 60-66. "[D]rain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed." '737 Patent at col. 3, lines 38-41. *See also* '737 Patent at col. 1, lines 14-29; col. 2, lines 10-14, 54-68; col. 3, lines 1-16, 24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d; and claim 1.		

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
at least a part of the mask	A "mask" is a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to material to be removed.	"Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6." '737 Patent at col. 2, lines 60-66. *See also* '737 Patent at col. 1, lines 14-29; col. 2, lines 10-14, 54-68; col. 3, lines 1-16,	At least a part of the layer which defines the edges of the selectively removed region.	*See support for claim term "said source and drain electrodes serving as at least a part of the mask" below.*

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d; and claim 1; USPN 4,331,758 to Luo issued May 25, 1982 at col. 5, lines 37-col. 6, line 7 (LPL Exh. 2). <u>Extrinsic Evidence:</u> *1988 Penguin* at 194 (defining "mask" as "A device used to shield selected areas of a semiconductor chip during the manufacture of semiconductor components and integrated circuits.) (LPL Exh. 5).		
said source and drain electrodes serving as at least a part of the mask	This phrase is a combination of previously defined constructions of	*See* definition of "source electrode", "drain electrode," and "at least a part of the	The source and drain electrodes make a significant contribution to	<u>Intrinsic Evidence</u>: "… [C]onducting film 30 and low-resistivity amorphous silicon

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	"source electrode", "drain electrode," and "at least a part of the mask", namely, the source and drain electrodes serve as at least part of the pattern placed above a surface from which material is to be selectively removed, where the pattern is made up of material that is resistive to the removal technique relative to material to be removed.	mask", *supra*.	defining the edges of the selectively removed region.	film 20 shown in FIG. 2c are selectively removed with said [drain and source] electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6." '737 Patent, col. 2 lines 60-66. *See also* '737 Patent, Figs. 1d, 2d, 3c; col. 4 lines 2-6. <u>Extrinsic Evidence</u>: U.S. Patent No. 5,905,274 to Ahn et al., Figs. 1E, 4E; col. 2 lines 32-39; col. 6 lines 55-61. Exh. 13. U.S. Patent No.

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				6,025,605 to Lyu, Figs. 2D, 3I; Col. 1 lines 60-64; col. 2 lines 49-52; col. 4 lines 8-12. Exh. 14.
"forming . . . on"	Providing . . . above and supported by or in contact with.	Intrinsic Evidence: '737 patent at col. 1, lines 14-17; col. 2, lines 8-17; Figs. 1a, 2a, 3a.	Giving form or shape to . . . above and supported by or in contact with.	Intrinsic Evidence: '737 patent, Figs. 2a-2e, 3a-3d; col. 1 lines 14-17, 21-31; col. 2 lines 8-35, 60-66; col. 3 lines 36-57.. Extrinsic Evidence: "Form" is defined as "to give form or shape to; to give a particular shape to; to serve to make up or constitute." *1981 Webster's* 447, Exh. 3.

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EXHIBIT E

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT E

U.S. Patent No. 5,825,449

CLAIM TERMS	AGREED CONSTRUCTION
"substrate"	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
"overlying"	Above.
"contact hole"	An opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.
"via hole"	An opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection between two metallization patterns.
"liquid crystal display device"	A type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel.
"material suitable for forming a pixel electrode"	A transparent, electrically conductive material that can be deposited and patterned, such as indium tin oxide (ITO).
"pixel electrode	A pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device.
"patterning"	The removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material.

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT E

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CLAIM TERMS	AGREED CONSTRUCTION
"insulative layer" and "insulating film"	A thickness of non-conductive material (such as SiNx) that has high electrical resistance.
"indium tin oxide layer"	A thickness of indium tin oxide (ITO).
"semiconductor layer"	A thickness of a semiconductor material, such as amorphous silicon.
"impurity-doped semiconductor layer"	A thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity.
"passivation layer"	A thickness of insulative material that provides protection such as electrical stability and chemical isolation.
"transparent conductive layer"	A thickness of transparent electrically conductive material.
conductive layer	A thickness of electrically conductive material.
one of a plurality of terminals of a thin film transistor	One of the terminals (i.e., source, drain, or gate) of a thin film transistor.

EXHIBIT F

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F
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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
on	Touching a top or side of. LPL believes this term has the same meaning as "formed on" and "disposed on", *infra*.	Intrinsic Evidence: '449 patent claims 1, 6, 8, 10, 11 (compare use of "on" with use of "overlying"). ". . . forming a first conductive layer pattern *on* a substrate . . . forming a second insulative layer *overlying* said substrate. . . ." Claim 8 (emphasis added). ". . . a source electrode and a drain electrode *on* said semiconductor layer . . . a passivation layer *overlying* said source pad. . . ." Claim 10 (emphasis added).	Above and supported by or in contact with.	Intrinsic Evidence: "As shown in FIG. 2c, a conductive layer for forming source electrode 7 and drain electrode 8 is deposited ***on*** the substrate by patterning a sputtered layer of conductive material." '449 Patent, col. 3 lines 63-66 (emphasis added). "As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited ***on*** the entire surface of the substrate by a CVD process." '449 Patent, col. 4 lines 6-8 (emphasis added). "As shown in FIG. 2e, an indium tin oxide

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		"... patterning said second conductive layer to form source electrode and a drain electrode *on* said active layer; forming a passivation film *overlying* said substrate including said source pad. . . ." Claim 11 (emphasis added). "An amorphous silicon active layer 4 is formed *on* a portion of gate insulating film 3 *overlying* gate 2." '449 patent at 1:42-44 (emphasis added.) *See also* '449 patent at 1:31-48, 56-64, 2:37-46, 3:44-62, 4:19-23,		(ITO) layer is next deposited ***on*** the substrate by sputtering or a CVD process ..." '449 Patent, col. 4 lines 16-19 (emphasis added). *See also* '449 Patent, Figs. 1-3, 5; Col. 1 lines 15-19, 34-64; col. 2 lines 5-13, 37-41, 56-67; col. 3 lines 44-66; col. 4 lines 39-41, 65-68; col. 5 lines 1-17; Claims 1, 2, 6, 8, 10, 11. <u>Extrinsic Evidence:</u> "On" is defined as "1.a. Used to indicate position above and supported by or in contact with: *The vase*

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		4:39-41, 4:65-5:7; Figs. 1a-f, 2a-e, 3; Claims 1, 2, 6, 8, 10, 11; '449 patent prosecution history, including Office Action of 8/1/97 at p. 2. <u>Extrinsic Evidence:</u> *1997 American Heritage Dictionary* at 953 (defining "on" as "[u]sed to indicate contact with or extent over (a surface) regardless of position") (LPL Exh. 5); *id.* at 974 (defining "overlie" as "to lie over or on"); *id.* at 972 (defining "over" as "[i]n or at a position above or higher than:		*is on the table.* b. Used to indicate contact with or extent over (a surface) regardless of position: *A picture on the wall.*" *The American Heritage College Dictionary* 953 (3d ed. 1997), Exh. 8. "On" is defined as "1. – Used to indicate: a. Position above and in contact with <The vase is *on* the bureau> b. Contact with a surface, regardless of position <a painting *on* the wall>." *Webster's II New College Dictionary* 764 (1995) ("*1995 Webster's*"), Exh. 6.

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		a sign over the door").		"Overlie" is defined as "to lie over or on" or "to lie over or upon." *The American Heritage College Dictionary* 974 (3d ed. 1997), Exh. 8; *1995 Webster's* 783, Exh. 6.
formed on	Touching a top or side of. LPL believes this term has the same meaning as "on", *supra*, and "disposed on", *infra*.	*See* support for claim term "on" *supra*.	Formed above and supported by or in contact with.	*See support for claim term "on" above.*
disposed on	Touching a top or side of. LPL believes this term has the same meaning as "on" and "formed on", *supra*.	*See* support for the term "on", *supra*.	Arrange above and supported by or in contact with.	*See support for claim term "on" above.* <u>Extrinsic Evidence</u>: "Dispose" is defined as "to arrange in a particular order". *1995 Webster's* 329, Exh. 6.
contact hole is	The contact hole is	<u>Intrinsic Evidence:</u>	A contact hole is made	<u>Intrinsic Evidence:</u>

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provided through . . . layer	formed in the layer.	Figs. 1b-1f, 2b-2e, 3-5; 1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47. *Compare* Claim 1 ("indium tin oxide layer extends through said first and second contact holes") *with* Figure 5 (showing indium tin oxide layer 6D entering one side of holes in insulative films 3 and 9 but not exiting out the opposite side).	in one side and out the opposite side.	'449 Patent, Figs. 1c-1f, 2d-2e, 3, 5 (showing contact holes made in one side and out the opposite side). *See also* '449 Patent, col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38. <u>Extrinsic Evidence</u>: "Through" is defined as "in one side and out the opposite or another side". *1995 Webster's* 1150 (1995), Exh. 6. *See also* agreed construction for "contact hole."
provided through	*See* definition of "contact hole is	*See* definition of "contact hole is	Made in one side and out the opposite side.	<u>Intrinsic Evidence:</u> '449 Patent, Figs. 1c-

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	provided through . . . layer", *supra*.	provided through . . . layer", *supra*.		1f, 2d-2e, 3, 5; Col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38. Extrinsic Evidence: "Through" is defined as "in one side and out the opposite or another side". *Webster's II New College Extrinsic Evidence* 1150 (1995) ("*1995 Webster's*"), Exh. 6. *See also* agreed construction for "contact hole."

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thin film transistor	A three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	<u>Intrinsic Evidence:</u> '449 patent at 1:22-33; Figs. 1-6. '449 patent prosecution history, including Amendment of 11/17/97 at p. 5 ("The terminals of a thin film transistor correspond to the gate, source, and drain.") (LPL Exh. 3). *See also* Amendment of 11/17/97 at pp. 2-7. <u>Extrinsic Evidence:</u> *1998 Penguin* 569 ("*thin-film transistor* (TFT) A MOSFET that is fabricated using thin-film techniques on an insulating substrate rather than	A semiconductor device in which the current flow between source electrode and drain electrode is controlled by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate.	<u>Intrinsic Evidence:</u> '449 Patent, Figs. 1-5; Col. 1 lines 13-33. <u>Extrinsic Evidence:</u> "Thin film technology" for circuits and systems is defined as "a technology in which a thin film (a few hundred to a few thousand angstroms in thickness) is applied by vacuum deposition to an insulating substrate". *1984 IEEE* 939, Exh. 2. Paul K. Weimer, *The TFT – A New Thin-Film Transistor* in *49 Proceedings of the IRE* 1462-64 (1962). Exh. 7.

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		on a semiconductor chip.") (LPL Exh. 6); *id*. at 205-207 ("*field-effect transistor* (FET) . . . It is a three terminal semiconductor device in which the current flow through one pair of terminals, the *source* and the *drain*, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by the voltage applied at the third terminal, the *gate*. . . ."); *id*. at 70 ("*chip* . . . A small piece of single crystal of semiconductor material containing		

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		either a single component or device or an integrated circuit.").		
selectively etching	Removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired	<u>Intrinsic Evidence:</u> '449 patent at 1:47-55, 2:8-10, 31-36. 50-51, 3:59-61, 3:67-4:1, 4:8-19, 35-39, 47-50, 5:1-15, 40-47; Figs. 1b-f, 2b-e, 3; Claims 8, 9, 11.	Having a selected portion of the substance of the first and second insulating layers removed using an etching technique.	<u>Intrinsic Evidence:</u> '449 Patent, Figs. 2d-2e, 3, 5; Col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38.

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	pattern on the surface.	Extrinsic Evidence: *1998 Penguin* at 190 (defining "etching" as "[c]hemical erosions of selected portions of a surface in order to produce a desired pattern on the surface.") (LPL Exh. 6). *Cf. id.* at 314-15 (defining "lift-off.").		
gate electrode	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.	Intrinsic Evidence: "[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1. "Referring first to	A conductive element of a single thin-film transistor that controls the current between source and drain by a voltage applied to its terminal. The gate electrode is distinct from the gate line and the gate pad associated with the gate electrode.	Intrinsic Evidence: "Referring first to FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used

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		FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device." '449 Patent, 3:44-49. *See also* '449 patent at 1:22-38, 56-60, 2:37-44, 2:56-61, 3:44-49, 4:47-53; 5:29-38; Figs. 1a-f, 2a-e, 3-6; Claims 10-11.		for applying a voltage in order to drive the active layer in the completed TFT device." '449 Patent, col. 3 lines 44-49. *See also* '449 Patent, Figs. 1-3, 5; col. 4, lines 50-53. <u>Extrinsic Evidence</u>: "Gate" is defined as a structural element of a TFT that "controls the current between source and drain by a voltage applied to its terminal". *1984 IEEE* 384, Exh. 2. "Gate" is defined as "[a]n electrode or electrodes in a field-

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				effect transistor." *The Penguin Dictionary of Electronics*, 237 (2nd. ed. 1988) ("*1988 Penguin*"), Exh. 10.
gate pad	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a gate driving circuit.	Intrinsic Evidence: "[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1. "[S]ource pad 2A is composed of gate	A portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array that is necessary to communicate information from an external driving circuit to a gate electrode.	Intrinsic Evidence: "Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively." '449 Patent, col. 1 lines 27-30. "Gate pad 2B is used for receiving a voltage to drive and active

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		material, as in the conventional method, and is formed at the same time as gate 2, storage capacitor electrode 2D and gate pad 2B." '449 patent at 4:51-53. *See also* '449 patent at 1:22-38, 1:52-60, 2:8-10, 2:19-26, 3:44-49, 4:6-14, 4:21-27, 4:35-41, 4:47-53, 4:65-5:1, 5:19-23; Figs. 1a-f, 3, 6; Claims 10-11. Extrinsic Evidence: *1998 Penguin* at 47 (defining "bonding pads" as "[m]etal pads arranged on a semiconductor chip (usually around the		layer in the completed TFT device." '449 Patent, col. 1 lines 34-38. "Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c)." '449 Patent, col. 1 lines 52-55. "Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched … thereby exposing … a

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		edge) to which wires may be bonded so that electrical connection can be made to the component(s) or circuit(s) on the chip.") (LPL Exh. 6).		predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C [sic]." '449 Patent, col. 4 lines 8-15. *See also* '449 Patent, Figs. 1-3, 5; Claims 10-11. <u>Extrinsic Evidence</u>: "Gate" is defined as the structural element of a thin film transistor that "controls the current between source and drain by a voltage applied to its terminal." *1984 IEEE* 384, Exh. 2.

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				European Patent No. 530834 to Matsuda, Figs. 1 and 3, Col. 4 lines 14-25, Exh. 9. *See also* support cited by LPL for the term "gad pad."
source pad	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a data driving circuit.	Intrinsic Evidence: "[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1. "[S]ource pad 2A is composed of gate material, as in the conventional method,	A portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array that is necessary to communicate information from an external driving circuit to a source electrode.	Intrinsic Evidence: "Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively." '449 Patent, Col. 1 lines 27-30. "Since a pad wiring layer is necessary in order to communicate information from an external driving circuit

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		and is formed at the same time as gate 2, storage capacitor electrode 2D and gate pad 2B." '449 patent at 4:51-53. *See also* '449 patent at 1:8-12, 1:22-38, 1:52-64, 2:8-10, 2:17-22, 3:66-4:5, 4:6-14, 4:24-27, 4:35-61, 4:65-5:1, 5:19-23, 5:48-51; Figs. 1a-f, 2d-e, 3, 6; Claims 10-11. <u>Extrinsic Evidence:</u> *1998 Penguin* at 47 (defining "bonding pads" as "[m]etal pads arranged on a semiconductor chip (usually around the edge) to which wires		to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c)." '449 Patent, col. 1 lines 52-55. "Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched … thereby exposing … a predetermined region of source pad 7A … For external electrical connections It is necessary to exposed pads 7A and 2C." '449 Patent, col. 4 lines 8-15. *See also* '449 Patent,

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		may be bonded so that electrical connection can be made to the component(s) or circuit(s) on the chip.") (LPL Exh. 6).		Figs. 1-3, 5; Claims 10-11. <u>Extrinsic Evidence</u>: "Source" is defined as the structural element of a thin film transistor that "contains the terminal from which charge carries flow into channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel". *1984 IEEE* 855, Exh. 2. European Patent No. 530834 to Matsuda, Figs. 1 and 3, Col. 4 lines 14-25, Exh 9. *See also* support cited

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				by LPL for the term "source pad."
gate insulating film	A thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor.	<u>Intrinsic Evidence:</u> '449 patent at 1:40:44, 1:52-55, 2:11-13, 2:19-26, 2:34-36, 2:40-44, 3:50-53, 4:1-15, 4:35-39, 4:47-50, 4:65-5:4, 5:12-15, 5:19-23, 5:40-46;	A thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the gate electrode from the semiconductor.	<u>Intrinsic Evidence:</u> '449 Patent, Figs. 1b-1f, 2b-2e, 3, 5; Col. 1 lines 39-41; col. 3 lines 50-52; col. 5 lines 1-4 <u>Extrinsic Evidence:</u> "Gate" is defined as the

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		Figs. 1b-f, 2b-e, 3, 5; Claim 10. <u>Extrinsic Evidence:</u> *1998 Penguin* at 209 (defining "film" as a "coating with a minimal thickness dimension.") (LPL Exh. 6). *1997 American Heritage Dictionary* at 770 (defining "layer" as a "thickness of material covering a surface or forming an overlying part or segment.") (LPL Exh. 5).		structural element of a thin film transistor that "controls the current between source and drain by a voltage applied to its terminal." *1984 IEEE* 384, Exh. 2. "Insulating material" is defined as "a substance or body, the conductivity or which is zero or, in practice, very small." *1984 IEEE* 447, Exh. 2. "Film" is defined as "a thin skin or membranous coating", "a thin coating". *1995 Webster's* 419, Exh. 6. "Layer" is defined as a

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				"thickness of material covering a surface or forming an overlying part or segment." *1997 American Heritage Dictionary* 770, LPL Exh. 5.
source electrode	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. Source electrode 7 is connected to source pad 2A, and drain electrode 8 is contact with impurity-doped	A conductive element of a single thin-film transistor formed over the source region from which charge carriers flow into the channel toward the drain. The source electrode is distinct from the source/data line and the source/data pad associated with the source electrode.	Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. … In the completed device structure, source electrode 7 conducts a data signal, received from a data wiring

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		semiconductor layer 5 and pixel electrode 6. In the completed device structure, source electrode 7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6. The signal is stored in the form of charge on pixel electrode 6, thereby driving the liquid crystal." '449 patent at 1:61-2:4. "[P]ortions of the impurity-doped semiconductor layer 5 are exposed and then etched. Source electrode 7 thus forms part of a transistor		layer and drain electrode 8, to pixel electrode 6." '449 Patent, col. 1 line 61 – col. 2 line 2. "As shown in FIG. 2c, a conductive layer for forming source electrode 7 and drain electrode 8 is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer 5 are exposed and then etched. Source electrode 7 thus forms part of a transistor

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		region and serves as source pad 7A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT." '449 patent at 3:67-4:5. "[S]ince both the first (45) and fourth (60) contact holes are formed over source pad 2A (formed of the same material as the gate) and source electrode 7, respectively, the source electrode 7 and source pad 2A may be connected to each other in the same step		region and serves as source pad 7A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT." '449 Patent, col. 3 line 63 – col. 4 line 5. "Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8." '449 Patent, col. 5 lines 6-8. *See also* '449 Patent,

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		that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer 6C connects source electrode 7 with source pad 2A, and a second transparent conductive layer 6 (i.e., the pixel electrode) is connected to drain electrode 8." '449 patent at 4:56-64. *See also* '449 patent 1:8-12, 1:22-30, 1:61-2:4, 2:11-27, 2:37-3:15, 3:63-4:5, 4:47-64, 5:6-15, 5:29-39, 5:48-54; Figs. 1e-f, 2c-e, 3-6, Claims 10, 11.		Figs. 1e-1f, 2c-2e, 3, 5; col. 1 lines 9-12; col. 2 lines 11-13. <u>Extrinsic Evidence</u>: "Source" is defined as a device structure which "contains the terminal from which charge carries flow into the channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel." *1984 IEEE* 855, Exh. 2. "Source" is defined as "[t]he electrode in a field-effect transistor that supplies charge carriers (holes or electrons) to the

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				interelectrode space." *1998 Penguin* 532, Exh. 10.
drain electrode	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. . . . In the completed device structure, source electrode 7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6. The	A conductive element of a single thin-film transistor formed over the drain region into which charge carriers flow from the source into the channel.	Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. … In the completed device structure, source electrode 7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6." '449

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		signal is stored in the form of charge on pixel electrode 6, thereby driving the liquid crystal." '449 patent at 1:61-2:4. *See also* '449 patent at 1:8-12, 1:22-30, 1:61-2:4, 2:11-27, 2:37-3:15, 3:63-4:5, 4:17-27, 4:47-64, 5:6-22; Figs. 1e-f, 2c-e, 3-6, Claims 10, 11.		Patent, col. 1 line 61 – col. 2 line 2. "Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8." '449 Patent, col. 5 lines 6-8. *See also* '449 Patent, Figs. 1e-1f, 2c-2e, 3, 5. <u>Extrinsic Evidence</u>: "Drain" is defined as a device structure which "contains the terminal into which charge carriers flow from the source into the channel.

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				It has the potential which is more attractive than the source for the carriers in the channel." *1984 IEEE* 276, Exh. 2. "Drain" is defined as "[t]he electrode of a field-effect transistor through which carriers leave the interelectrode space." *1998 Penguin* 152, Exh. 10.
active layer	A discrete portion of the semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the	<u>Intrinsic Evidence:</u> '449 patent at 1:34-51, 1:61-2:4, 2:11-27, 3:44-62, 4:65-5:5, 5:39-47; Figs. 1b-f, 2b-e, 3, 5; Claim 11. <u>Extrinsic Evidence:</u> *1997 American*	A thickness composed of a semiconductor material through which charge carriers flow between a source region and drain region.	<u>Intrinsic Evidence:</u> '449 Patent, Figs 1-3, 5; Col. 1 lines 41-50; col. 3 lines 53-62; col. 5 lines 1-5. <u>Extrinsic Evidence:</u> "Layer" is defined as a "thickness of material

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
	electric field introduced by the gate electrode.	*Heritage Dictionary* at 770 (defining "layer" as a "thickness of material covering a surface or forming an overlying part or segment.") (LPL Exh. 5).		covering a surface or forming an overlying part or segment." *1997 American Heritage Dictionary* 770, LPL Exh. 5.
common hole	A shared hole.	Intrinsic Evidence: '449 patent at 4:47-64; 5:8-22, 33-38; Figs. 3, 5; claim 4. Extrinsic Evidence: *1997 American Heritage Dictionary* at 281 (defining "common" as "[b]elonging equally to or shared equally by two or more; joint.") (LPL Exh. 5).	A single hole.	Intrinsic Evidence: '449 Patent, Figs. 3, 5; Col. 4 lines 47-64; col. 5 lines 8-22, 33-38. Extrinsic Evidence: "Common" is defined as "belonging to, shared by, or applying equally" *1995 Webster's* 226. Exh 2.
aligned	Placed in line with.	Intrinsic Evidence: '449 patent at 4:47-64;	Substantially co-axial or concentric.	Intrinsic Evidence: '449 Patent, Figs. 3, 5;

1-LA/750423.1

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F
U.S. Patent No. 5,825,449

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		5:8-22, 33-38; Figs. 3, 5; claim 5. <u>Extrinsic Evidence:</u> *1997 American Heritage Dictionary* at 34 (defining "align" as "[t]o arrange in a line. . . .") (LPL Exh. 5).		Col. 4 lines 47-64; col. 5 lines 8-22, 33-38. <u>Extrinsic Evidence:</u> "Align" is defined as "to place in a line." *1995 Webster's* 28. Exh. 2.
said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region	The second insulating layer includes "a second contact hole" that exposes a portion of the second conductive layer. The second insulating layer also includes "said first contact hole region", <u>i.e.</u>, it includes part of the first contact hole which exposes the predetermined portion	<u>Intrinsic Evidence:</u> '449 patent at 2:37-55; 3:2-14; 4:47-64; 5:8-22, 33-38; Figs. 3, 5; claims 1, 2, 5, 6, 8, 10, and 11.	The second deposited layer of insulating material has a second contact hole through it which: (a) uncovers a selected portion of the second deposited conductive layer and (b) uncovers the region in which the first contact hole is located. The first and second contact holes must overlap.	<u>Intrinsic Evidence:</u> '449 Patent, Figs. 3, 5; Col. 4 lines 47-64; col. 5 lines 8-22, 33-38.

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F
U.S. Patent No. 5,825,449

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
	of the first conductive layer.			
wiring structure	A slender structure electrically connecting at least two points.	Intrinsic Evidence: '449 patent at 4:24-27. Extrinsic Evidence: *1997 American Heritage Dictionary* at 1547-1548 (defining "wire" as "resembling a wire, as in slenderness") (LPL Exh. 5).	A structure providing an electrically conductive path that connects at least two terminals.	Intrinsic Evidence: "The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed." '449 Patent, Col. 4 lines 24-26; Figs. 1-5. *See also* '449 Patent, Col. 1 lines 52-55; col. 2 lines 1, 16-18; col. 4 lines 1-5.

PROOF OF SERVICE

I am a resident of the State of California and over the age of eighteen years, and not a party to the within action; my business address is 300 South Grand Avenue, Twenty-Second Floor, Los Angeles, California 90071-3132.

On December 23, 2003, I served the within document(s):

SECOND REVISED JOINT CLAIM CONSTRUCTION STATEMENT

☐ by transmitting via facsimile the document(s) listed above to the fax number(s) set forth below on this date before 5:00 p.m.

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I declare that I am employed in the office of a member of the bar of this court at whose direction the service was made.

CCMamayson

Catherine C. Mamayson

1-LA/750383.1

EXHIBIT C-7

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UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

CIVIL MINUTES--GENERAL

Case No. CV 02-6775 CBM (JTLx)

Date: October 19, 2006

Title: LG. Philips LCD Co., Ltd. v. Chunghwa Picture Tubes, Ltd., et al.

DOCKET ENTRY
ORDER CONSTRUING TERM "ONE" AS FOUND IN CLAIM ONE OF U.S. PATENT NO. 5,825,449

PRESENT: Hon. CONSUELO B. MARSHALL, JUDGE

JOSEPH LEVARIO	N/A
Deputy Clerk	Court Reporter

ATTORNEYS PRESENT FOR PLAINTIFFS: N/A

ATTORNEYS PRESENT FOR DEFENDANTS: N/A

PROCEEDINGS:

The matter before the Court is the parties' dispute over the proper construction over the term "one" as found in Claim 1 of U.S. Patent No. 5,825,449 (the '449 Patent).

In a bench brief filed with this Court, Defendant requests that the Court construe the language of Claim 1 of the '449 Patent as open-ended, meaning that the term "reads on products that have one or more conductive layers connected to one of a plurality of terminals of a thin film transistor." Def.'s Br. 1. The relevant claim language is:

> A wiring structure comprising:
> a substrate;
> a first conductive layer formed on a first portion of said substrate;
> a first insulative layer formed on a second portion of said substrate and on said first conductive layer;
> a second conductive layer formed on a first portion of said first insulative layer;
> [. . .]
> wherein a first contact hole is provided through said first and second insulative layers . . .

and

> *wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.*

'449 Patent (emphasis added). Defendant seeks to have this Court interpret the last phrase beginning with "wherein one of said first and second conductive layers . . . ." Plaintiff LG.Philips argues that the phrase "one of" should be construed as "one, but not both, of the first and second conductive layers." Pl.'s Mem. 1.

Claim construction is a matter of law, and it is the duty of this Court to construe disputed

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claim terms and instruct the jury as to its meaning. *See* Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996).

The Federal Circuit has held that a court construing a claim must give effect to the intent of the patent applicant. *See* Lemelson v. General Mills, Inc., 968 F.2d 1202, 1206 (Fed. Cir. 1992). ("The prosecution history gives insight into what the applicant originally claimed as the invention, and often what the applicant gave up in order to meet the Examiner's objections."); *see also* Standard Oil Co. v. American Cyanamid Co., 774 F.2d 448, 452 (Fed. Cir. 1985) ("The prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance."). In the instant case, patentee LG Electronics specifically disavowed an interpretation of the claim that provided for either, or both - in other words, "one or more" - of the conductive layers being connected to a terminal of a thin film transistor; in December 1997, in order to obviate an obviousness rejection, LGE patent applicant Woo Sup Shin specifically amended the claim to articulate the "one of said first and second layers" limitation. The Court, therefore, finds that the term "one" in Claim 1 means "a single layer."

Accordingly, the Court adopts Plaintiff LG.Philips' interpretation of the relevant language in Claim 1 of the '449 Patent:

The phrase "one of" in the "wherein one of said first and second conductive layers" limitation means one, but not both, of the first and second conductive layers."

IT IS SO ORDERED.

Initials of Deputy Clerk ___

cc: Judge Marshall
Parties of Record

EXHIBIT C-8

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LOS ANGELES
BY

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

LG.PHILIPS LCD CO., Ltd.,

Plaintiff,

vs.

TATUNG CO. OF AMERICA, et al.,

Defendants.

AND COUNTERCLAIMS

Case No. 02-6775 CBM (JTLx)

[Related Case Nos. CV-03-2866 CBM, CV-03-2884 CBM, CV-03-2885 CBM and CV-03-2886 CBM]

MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT OF LG.PHILIPS LCD CO., LTD.'S RENEWED MOTION FOR JUDGMENT AS A MATTER OF LAW THAT DEFENDANTS INFRINGE CLAIMS 10-11 OF THE '449 PATENT

Judge: Hon. Consuelo B. Marshall
Courtroom: 2
Date: March 12, 2007
Time: 10:00 am

PUBLIC VERSION

DOCKETED ON CM
JAN 18 2007
BY

1-WA/2685569.1

(153)

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I. INTRODUCTION

Pursuant to Federal Rule of Civil Procedure 50(b), LG.Philips LCD Co., Ltd. ("LG.Philips") renews its motion for judgment as a matter of law that defendants infringe claims 10 and 11 of U.S. Patent No. 5,825,449 ("the '449 patent"), Roth Decl., Ex. 1.

On November 21, 2006, the jury returned a verdict that defendants willfully infringe claim 1 of both the '449 and '737 patents. However, the jury found that claims 10 and 11 of the '449 patent were not infringed. Notwithstanding this verdict, and as requested in LG.Philips' November 8 motion for judgment as a matter of law (Docket Entry 1426), the Court should enter judgment of infringement on these claims.

Infringement analysis involves two steps. First, the claims are construed by the court. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1454 (Fed. Cir. 1998) (en banc). Second, the properly construed claims are compared to the accused device to determine infringement. *Id.* Here, the Court construed claims 10 and 11. When this construction is applied to defendants' products, there is plain and indisputable infringement. At trial, defendants did not contest that they used virtually all of the features of claims 10 and 11. Defendants' purported "defense" was that their products did not include the "source pad" required by the claims. However, defendants' expert admitted that the accused products include a structure with each of the features required by the Court's construction of "source pad." Hence, the undisputed evidence compels a conclusion of infringement.[1]

II. LEGAL STANDARD

A motion for judgment as a matter of law made prior to the case being submitted to the jury may be renewed after the verdict pursuant to Federal Rule of

[1] References to the Trial Transcript ("Trial Tr.") in this memorandum, as well as LG.Philips' other post-verdict memoranda, are collected as a single exhibit to the Declaration of David M. Morris in Support of Post-Verdict Motions of LG.Philips LCD Co., Ltd.

Civil Procedure 50(b). Such motions may be granted against a party if "the court finds that a reasonable jury would not have a legally sufficient evidentiary basis to find for the party on that issue." Fed. R. Civ. P. 50(a).

III. ARGUMENT

A. THE UNDISPUTED FACTS COMPEL A FINDING OF INFRINGEMENT OF CLAIMS 10 AND 11 OF THE '449 PATENT

LG.Philips' renewed motion turns on a narrow issue – whether the accused products include the "source pad" recited in claims 10 and 11 of the '449 patent.[2] The relevant facts – *i.e.*, the structure of the "source pad" – are not in dispute and, therefore, the issue is amenable to resolution on motion for judgment as a matter of law. *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 and 250 (1986); *Gentry Gallery, Inc. v. Berkline Corp.*, 134 F.3d 1473, 1476 (Fed. Cir. 1998) ("Because there is no dispute concerning the structure of the accused device, our infringement analysis involves only claim construction, a question of law . . . .").

Claim 10 calls for a "first conductive layer" that includes a "source pad," and claim 11 similarly calls for "patterning said first conductive layer to form . . . a source pad." Defendants admit that their products include a "source pad," but dispute that the "source pad" is in the "first conductive layer." Instead, they

[2] Defendants also argued that the accused products do not include two other claim limitations: *i.e.*, the "first contact hole … exposing said source pad" limitation and the "transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact holes" limitation. However, as defendants acknowledge, these arguments are dependent upon the "first conductive layer" not containing a "source pad." CPT JMOL Motion at 6:3-12, Nov. 9, 2006, Docket Entry 1415. If the "first conductive layer" in defendants' products includes the "source pad" identified by LG.Philips, then these limitations are satisfied. Defendants did not contest the remaining limitations – the testimony of Dr. Rubloff, LG.Philips' expert, is unrebutted. *See, e.g.*, Trial Tr. at 1183:22-1186:17, 1193:6-1193:16, 1194:9-1195:14. Moreover, defendants eventually conceded that they imported into the United States or sold or offered for sale in the United States accused products, (*id.* at 927:6-928:5, 929:18-931:13, 1837:24-1842:6; Roth Decl., Exs. 2-9); and the jury necessarily found that defendants induced infringement of the '449 patent. As a result, if the accused products include the "source pad" limitation, then defendants infringe.

contend that the material LG.Philips identifies as the first conductive layer "source pad" is a The structure in question is illustrated below in red as the "First Metal Layer."[3]

The Court's construction of "source pad" – an issue of law – resolves the dispute. The jury was instructed that "source pad" means "a portion of a patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a data driving circuit." Roth Decl., Ex. 10.

There is no dispute that the accused products include a material in the – *i.e.*, the material shown in red in the above illustration – meeting this definition. LG.Philips' expert, Dr. Rubloff, testified that this is so. Trial Tr. at 1182:13-1183:21, 1187:8-15, 1188:17-25, 1190:4-23, 1193:17-1194:11, 3102:19-3111:18, and 3119:5-3130:7. Defendants' expert concurred. He admitted that the portion of the illustrated above:

- is patterned, *id.* at 2792:17-19;
- is electrically conductive, *id.* at 2792:17-19;
- is provided near the periphery of the TFT array, *id.* at 2793:10-14;

[3] This illustration is taken from defendants' and their expert's demonstratives used at trial. Trial Tr. at 1982:5-15 and 2687:8-18.

- receives a voltage (*i.e.*, "data")[4] from the source driver, *id.* at 1996:10-14 and 2800:2-5; and
- receives a current, *id.* at 2801:4-5.

In short, Defendants' expert admitted that the first metal identified by LG.Philips includes each feature required by the Court's definition of "source pad." Therefore, the undisputed facts demonstrate that the accused products include the "source pad" recited in claims 10 and 11 of the '449 patent. Judgment of infringement of claims 10 and 11 should be entered.

B. DEFENDANTS' ARGUMENTS THAT THEIR PRODUCTS DO NOT CONTAIN A FIRST METAL SOURCE PAD ARE BASED ON IRRELEVANT OR NON-EXISTENT EVIDENCE

Defendants presented two arguments why the accused products allegedly do not include the claimed "source pad." The first argument is based upon irrelevant evidence; the second on imaginary evidence.

First, defendants argued that the "source pad" is a But the name allegedly used to describe the first metal in CPT's products has no bearing on whether the piece of metal meets the Court's definition of "source pad." If it did, then infringement could easily be avoided merely by assigning names to the electrical components different from those used in the patent. The undisputed evidence – including the admissions from defendants' expert – demonstrates that the first metal identified by LG.Philips in the accused products includes each of the features described by the Court. Indeed, the metal is labeled as part of the "Source" in CPT's engineering documents. *See, e.g.*, Roth Decl., Exs. 11 and 12.

Second, defendants argued that no "data" is received by the relevant portion of the first metal and, therefore, it cannot be a source pad. This argument is

---

4 Defendants' expert testified by deposition in 2005 that the "data" from the data driving circuit is represented as a voltage. Trial Tr. at 2794:2-2795:8, 2795:24-2796:17.

contrary to the undisputed facts. As illustrated below, the data driving circuit, which applies the "data," Trial Tr. at 2793:21-23, is electrically connected to the second metal layer. Defendants concede that this second metal layer receives data – they refer to the second metal layer shown below as the source pad, which by definition receives data. *Id.* at 2688:5-15. Hence, because the first metal layer is

Defendants' expert agreed. He admitted that the (*i.e.*, "source pad") receives virtually the same voltage from the data driving circuit as the second metal layer. Trial Tr. at 2799:12-2800:5. Mr. Hsu, the only CPT engineer called by defendants at trial, also admitted that *Id.* at 1996:11-14. Defendants' expert also admitted in his deposition in 2005 that he agrees with LG.Philips' expert, Dr. Rubloff, that voltage represents data. *Id.* at 2794:2-2795:8, 2795:24-2796:17. At trial defendants' expert attempted to backtrack from this admission, arguing that current also was needed. *Id.* at 2793:24-2794:1, 2795:13-22, 2796:16-21. However, on cross-examination, he conceded that the also received current. *Id.* at 2801:4-5.

In short, the first metal layer illustrated above receives the same data The portion of the first metal layer identified by LG.Philips meets the Court's definition of source pad.

IV. CONCLUSION

For the foregoing reasons, LG.Philips requests that the Court enter judgment as a matter of law that defendants infringe claims 10 and 11 of the '449 patent.

Dated: January 16, 2007

MORGAN, LEWIS & BOCKIUS LLP

By Anthony C. Roth
Anthony C. Roth
Attorney for LG.Philips LCD Co., Ltd.

EXHIBIT E-2

PATENT
ATTORNEY DOCKET NO.: 041501-5507

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Confirmation No.: 6516
Sang Ho PARK, et al.	Group Art Unit: 2871
Application No.: 10/128,452	Examiner: T. Chowdhury
Filed: April 24, 2002	
For: METHOD AND APPARATUS FOR MANUFACTURING LIQUID CRYSTAL DISPLAY DEVICE USING SERIAL PRODUCTION PROCESSES (As Amended)	

Commissioner for Patents
U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

AMENDMENT

In response to the Office Action dated October 6, 2003, the period for response to which extends through January 6, 2004, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title of the invention to read as follows:

METHOD AND APPARATUS FOR MANUFACTURING LIQUID CRYSTAL DISPLAY DEVICE USING SERIAL PRODUCTION PROCESSES

REMARKS

Summary of the Office Action

The title of the invention stands objected to as allegedly not being descriptive.

Claims 1-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' allegedly admitted prior art (AAAPA) in view of JP 08-171076 (JP076).

Summary of the Response to the Office Action

Applicants have amended the title of the invention. Claims 1-21 are presently pending. In addition, Applicants provide herewith a machine translation of JP 08-171076 from the JPO website.

The Objections to the Title of the Invention

The title of the invention stands objected to as allegedly not being descriptive. Applicants have amended the title of the invention in accordance with the comments of the Examiner. Accordingly, Applicants respectfully request that the objection to the title of the invention be withdrawn.

The Rejection under 35 U.S.C. § 103(a)

Claims 1-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' allegedly admitted prior art (AAAPA) in view of JP 08-171076 (JP076). Applicants respectfully assert that the claims are allowable for at least the following reasons.

With respect to independent claim 1, Applicants respectfully assert that AAAPA and JP076, whether taken singly or combined, do not teach or suggest a combination including passing the first and second substrates through a sealing material coating portion of the single

production process line in serial order such that a sealing material is coated on the second substrate and the first substrate is passed through the sealing material coating portion without forming a sealing material thereon. Similarly, Applicants respectfully assert that AAAPA and JP076, whether taken singly or combined, do not teach or suggest a combination including passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order such that liquid crystal is dispensed onto a pixel region of one of the first and second substrates and the other one of the first and second substrates is passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon.

In AAAPA, Applicants respectfully assert that if a substrate passes through a process portion, the corresponding process is always performed. Thus, no substrate would be passed through a sealing material coating portion without forming a sealing material thereon. Similarly, no substrate would be passed through a liquid crystal dispensing portion without dispensing liquid crystal thereon. The Office Action appears to recognize this deficiency and, therefore, further relies on JP076 for an alleged teaching of using a single production line.

However, Applicants respectfully assert that if a substrate passes through a process portion in JP076, the corresponding process is always performed. Specifically, at paragraph [0023], JP076 teaches that parallel processing is carried out on each distinguished substrate with separate lines when distinct processes are desired whereas a common processing is carried out on the substrates when the same processes are desired. Thus, in JP076 like AAAPA, no substrate would be passed through a sealing material coating portion without forming a

sealing material thereon. Similarly, no substrate would be passed through a liquid crystal dispensing portion without dispensing liquid crystal thereon. In other words, Applicants respectfully assert that JP076 not only fails to remedy the deficiencies of AAAPA but also that JP076 teaches away from using a single production line when distinct processes are desired for each type of substrate. As a result, Applicants respectfully assert that the rejection of independent claim 1 is improper and that independent claim 1 is allowable.

In addition to the arguments provided above, Applicants respectfully note that JP076 relates to processes for washing, exposing and developing, and lacks teachings relating to sealing material coating or to LC dispensing. Accordingly, Applicants respectfully assert that JP076 cannot be used to provide any teaching or suggestion relating to sealing material coating or to LC dispensing. Thus, Applicants respectfully assert that the application of JP076 is improper.

Applicants respectfully assert that the rejections of independent claims 14 and 21 are improper and that independent claims 14 and 21 are allowable at least for reasons similar to those set forth above with respect to independent claim 1.

Applicants respectfully assert that dependent claims 2-13 and 15-20 are allowable at least because of their dependency from independent claims 1 and 14, and the reasons set forth above.

Conclusion

Applicants respectfully request reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

1-WA/2077697.1

If there are any fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted

MORGAN, LEWIS & BOCKIUS LLP

By: ______________________
Robert J. Goodell
Reg. No. 41,040

Dated: January 6, 2004

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1-WA/2077697.1

EXHIBIT E-3

Webster's Third New International Dictionary

OF THE ENGLISH LANGUAGE

UNABRIDGED

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Webster's third new international dictionary of
the English language, unabridged.

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MADE IN THE UNITED STATES OF AMERICA

41KP88

sinch *var of* CINCH

sin·cip·i·tal \(ˈ)sin¦sipəd·ᵊl\ *adj* [L *sincipit-, sinciput* + E *-al*] **:** of or relating to the sinciput

sin·ci·put \ˈsin(t)sə(ˌ)pət, *usu* -əd·+V\ *n, pl* **sinciputs** \-ts\ *or* **sin·cip·i·ta** \sinˈsipəd·ə\ [L, fr. *semi-* + *caput* head — more at HEAD] **:** a part of the head: **a :** FOREHEAD **b :** the whole upper half of the skull **:** CALVA **c :** the forepart of the head of a bird from the base of the bill to the crown **d :** the part of the head of an insect and esp. of a beetle between the vertex and the clypeus

sin·cos·ite \ˈsiŋkəˌsīt\ *n* -s [*Sincos*, Peru, where it was discovered + E *-ite*] **:** a mineral $Ca(VO)_2(PO_4)_2.5H_2O$ consisting of hydrous calcium vanadyl phosphate and occurring in thin tetragonal scales or plates

sind \ˈsin(d), ˈsīn\ *vt* [ME (Sc & northern dial.) *sinden*] *chiefly Scot* **1 :** to rinse out **2 :** to wash down (food)

sin·der \ˈsində(r), ˈsinər\ *chiefly Scot var of* SUNDER

sin·dhi \ˈsindē\ *n* [Ar *Sindi*, fr. *Sind* Sind, Sindh, region in the northwestern part of the Indian subcontinent, fr. Hindi; akin to Skt *sindhu* river — more at INDIA] **1** *also* **sin·di** \"\ *pl* **sindhi** *or* **sindhis** *also* **sindi** *or* **sindis** *usu cap* **a :** a Scytho-Dravidian mostly Muslim people of Sind **b :** a member of such people **2** *pl* **sindhi** *or* **sindhis** *usu cap* **:** the Indic language of Sind **3 a** *usu cap* **:** an Indian breed of dark red short-horned humped dairy cattle that is widely distributed and much used for crossbreeding in warm regions **b** *pl* **sindhi** *or* **sindhis** *often cap* **:** an animal of the Sindhi breed

sind ibex \ˈsind-\ *n, usu cap S* [*sind* fr. *Sind*, region in the northwestern part of the Indian subcontinent] **:** a wild goat (*Capra hircus blythi*) of Sind and Baluchistan

sin·di·co \ˈsēndəˌkō\ *n* -s [Sp, fr. LL *syndicus* — more at SYNDIC] **:** SYNDIC

sin·don \ˈsindən\ *n* -s [ME, fr. L, fr. Gk *sindōn*] **1** *archaic* **:** a fine fabric esp. of linen **2** *archaic* **:** a covering made of sindon: as **a :** SHROUD ⟨Christ's ~⟩ **b :** ¹CORPORAL

sin·dry \sindri\ *chiefly Scot var of* SUNDRY

sine \ˈsīn\ *n* -s [ML *sinus* (intended, under influence of Ar *jaib* curve, as trans. of Ar *jiba* sine, fr. Skt *jīva* bowstring, chord of an arc), fr. L, curve, fold — more at SINUS] **:** the *y* coordinate of any point except the vertex on the terminal side of an angle divided by the distance between the vertex and the point, the vertex coinciding with the origin of a plane rectangular coordinate system and the initial side of the angle coinciding with the positive x-axis

sin–eater \ˈ≈ˌ≈≈\ *n* **:** a person formerly hired to assume the sins of a dead person by eating food placed near the corpse

sin–eating \ˈ≈ˌ≈≈\ *n* **:** the act or practice of a sin-eater

sine bar *n* **:** a device that consists of a steel straightedge at whose extremities buttons are attached with their centers equidistant from the straightedge and that is used to locate work at desired angles on angle plates

¹**si·ne·cure** \ˈsīnəˌkyů(ə)r, ˈsin-, -nēˌ-, -ůə\ *n* -s [ML (*beneficium*) *sine cura* (benefice) without cure of souls] **1 :** an ecclesiastical benefice without cure of souls **2 :** an office or position that requires little or no work and that usu. provides an income

²**sinecure** \"\ *adj* **:** having the characteristics of a sinecure ⟨a practically ~ office —Valentine Heywood⟩

sine·cur·ism \-ˌrizəm\ *n* -s **:** the practice of granting sinecures

sine·cur·ist \-ˌrəst\ *n* -s **:** one who has a sinecure

sine curve *n* **:** the graph in rectangular coordinates of the equation $y = a \sin bx$ where *a* and *b* are constants that when $a = 1$ and $b = 1$ passes through the origin and all points on the x-axis where the abscissas are multiples of π radians, is concave towards the x-axis, and has maximum and minimum ordinate values of +1 and −1

¹**sine die** \ˌsīnēˈdīˌē, -nəˈd-, ÷ -dī *also* ˌsin-; ˌsi(ˌ)nāˈdēˌā, ˌsē, ˌnēˈd-, ˌnəˈd-, -dīˌā\ *adv* [L] **:** without any future date being designated (as for resumption) **:** INDEFINITELY ⟨declared the House adjourned *sine die* —Holding Carter⟩

²**sine die** \"\ *adj* **:** made without any date being designated (as for resumption) **:** INDEFINITE ⟨favored an adjournment *sine die* of Congress⟩

sine law *n* **:** LAW OF SINES

sine plate *n* **:** a block or plate for holding parts for machining at desired angles

sine pro·le \ˌsīnēˈprōˌlē, ˌsin-, -nəˈp-; ˌsi(ˌ)nāˈprō(ˌ)lā, ˌsē, ˌnēˈp-, ˌnəˈp-\ *adv* [L] **:** without issue ⟨died *sine prole* in his 80th year⟩

¹**sine qua non** \ˌsi(ˌ)nāˌkwäˈnōn, ˌsē, ˌnēk-, ˌnəˌk-, -ˈnän; ˌsīnēˌkwāˈnän, -ˌīnəˌk- *also* ˌsin-\ *n, pl* **sine qua nons** [LL, lit., without which not] **1 :** the one thing that is absolutely essential ⟨the *sine qua non* ... is that the star shall appear bright enough to give a measurable spectrum —Herbert Dingle⟩ **2 :** something that is considered essential ⟨this book is a *sine qua non* for Mill scholars —W.D.Templeman⟩

²**sine qua non** \"\ *adj* **:** absolutely necessary **:** ESSENTIAL, INDISPENSABLE ⟨wider spaced patterns are ... *sine qua non* in men's wardrobes —*N.Y.Times*⟩ ⟨it's the *sine qua non* sense —Amy Lowell⟩

sinetic *usu cap, var of* SINITIC

¹**sin·ew** \ˈsi(ˌ)nyü *also* ÷ ˈsi(ˌ)nü\ *n* -s [ME *sinwe, senewe*, fr. OE *sinu, seonu*; akin to MD *senewe* sinew, OHG *senawa*, ON *sin* sinew, MIr *sin* chain, L *seta, saeta* bristle, Gk *himas* leather strap, thong, Skt *syati, sinati* he binds, straps] **1 :** TENDON; *esp* **:** one dressed for use as a cord or thread ⟨his linden cradle ... safely bound with reindeer ~s —H.W.Longfellow⟩ **2** *obs* **:** NERVE **3 a :** solid resilient strength **:** POWER, FORCE ⟨to espouse democratic government demands intellectual and moral ~ as well as armies and good feeling —G.K.Chalmers⟩ ⟨a solidly constructed novel, a tale with thews and ~s —William McFee⟩ **b :** the chief supporting force **:** MAINSTAY — usu. used in pl. ⟨equipment ... providing the ~s of better living —Sam Pollock⟩ **c :** financial or material resources — usu. used in the phrase *sinews of war*

²**sinew** \"\ *vt* -ED/-ING/-S **1 :** to run through as if with sinews in order to make strong ⟨no ordinary belt ... because it is ~ed with finely stranded airplane-type steel cables —*Newsweek*⟩ **2 :** to give force or solidity to **:** STRENGTHEN ⟨serve to ~ the state in times of danger —Oliver Goldsmith⟩

sine wave *n* **:** a fundamental form of wave (as in one of the sound waves giving rise to a pure tone or in a wave of alternating current) that represents periodic oscillations in which the amplitude of displacement at each point is proportional to the sine of the phase angle of the displacement and that is visualized as a sine curve

sinew–backed bow \ˈ≈(ˌ)≈ˌ≈-\ *n* **:** REINFORCED BOW

sin·ewed \ˈsi(ˌ)nyüd *also* ÷ ˈsi(ˌ)nüd\ *adj* [¹*sinew* + *-ed*] **:** having sinews **:** SINEWY

sin·ew·i·ness \ˈsin(y)əwēnəs, -win-\ *n* -ES **:** the state or quality of being sinewy

sin·ew·less \ˈ≈(ˌ)≈ləs\ *adj* **:** having no sinews

sin·ew·ous \ˈsin(y)əwəs\ *adj* **:** SINEWY

sin·ewy \-(y)əwē, -wi\ *adj* [ME *senewy*, fr. *senewe* sinew + *-y*] **1 :** having sinews: **a :** full of sinews **:** TENDINOUS ⟨the ~ parts of a cut of meat⟩ **b :** marked by strong or prominent sinews ⟨~ arms rising and falling in tireless unison —T.B. Costain⟩ **2 :** marked by the strength of sinews **:** strong and firm **:** TOUGH ⟨putting down the sum of his experience in his rich ~ prose —Cyril Connolly⟩ ⟨bitter and ~ intellectuality —Robert Halsband⟩

sin·fo·nia \ˌsinfəˈnēə, -imf-\ *n, pl* **sinfo·nie** \-ēˌā\ [It, symphony, sinfonia, fr. L *symphonia* — more at SYMPHONY] **1 :** an orchestral musical composition of Italian origin found in 18th century opera or other vocal composition **:** OVERTURE **2 :** SYMPHONY 2

sin·fo·nie \ˌzinfəˈnē, ˌsi-\ *n, pl* **sinfoni·en** \ˌ≈≈ˈnēən\ *usu cap* [G, fr. It *sinfonia*] **:** SYMPHONY

sin·fo·niet·ta \ˌsinfənˈyed·ə, -fōn-, -eto\ *n* -s [It, dim. of *sinfonia* symphony] **1 :** a symphony of less than standard length or for fewer instruments **2 :** a small symphony orchestra; *esp* **:** an orchestra of strings only

sin·ful \ˈsinfəl\ *adj* [ME, fr. OE *synfull*, fr. *syn* sin + *-full* -ful — more at SIN] **1 :** tainted with or full of sin **:** WICKED, INIQUITOUS ⟨~ men⟩ **2 :** marked by or involving sin ⟨~ thoughts⟩ ⟨~ practices⟩ **3 :** highly culpable ⟨a ~ waste in a world that lacks a sufficiency of food —Lionel Trilling⟩

sin·ful·ly \-fəlē, -li\ *adv* [ME, fr. *sinful* + *-ly*] **1 :** in a sinful manner **:** WICKEDLY **2 :** CULPABLY, UNREASONABLY ⟨cars can be hired at a ~ high price —T.H.Fielding⟩

sin·ful·ness \-lnəs\ *n* -ES [ME *sinfulnesse*, fr. *sinful* + *-nesse* -ness] **:** the quality or state of being sinful ⟨man of moderate intelligence and normal ~ —R.H.Rovere⟩

¹**sing** \ˈsiŋ\ *vb* **sang** \ˈsaŋ, -aiŋ\ *or* **sung** \ˈsəŋ\ **sung** *also* **sang**; **singing**; **sings** [ME *singen*, fr. OE *singan*; akin to OHG *singan* to sing, ON *syngja*, Goth *siggwan* to sing, MW *deongl* to explain, Gk *omphē* voice, oracle and prob. to Prakrit *samghai* to say, teach] *vi* **1 a :** to produce musical tones by means of the voice **b :** to utter words in musical tones and with musical inflections and modulations ⟨to ~ at one's work⟩ ⟨children that dance and ~⟩ **c :** to produce in a proper or skilled manner tones generated by vibrations of the vocal cords and resonated by the various oral cavities; *also* **:** to deliver songs, arias, or other compositions in the character of a trained or professional singer ⟨~ extremely well⟩ ⟨~ for charity or in opera⟩ **2 :** to make a shrill whining or whistling sound ⟨a kettle ~ing on the hearth —Elizabeth Goudge⟩ ⟨the high overtone of the saw ... ~ing when it runs free —*Amer. Guide Series: Ark.*⟩ ⟨bullets hit the road surface and *sung* off —Ernest Hemingway⟩ **3 a :** to relate, describe, or celebrate something in verse ⟨~s of Arthur and his Knights of the Round Table⟩ ⟨poets *sang* of the natural man —*Amer. Guide Series: Minn.*⟩ ⟨gave substance and reality to the beauty of which he *sang* —H.M.Reynolds⟩ **b :** to compose poetry **:** make verse ⟨it was blank verse that she *sang* —Virginia Woolf⟩ **c :** to convey in or through words a feeling or sense of rhythm ⟨writes a prose remarkable for its live and lyric qualities; she makes the language ~ —Charles Lee⟩ ⟨the second means of writing prose that ~s is to train yourself to feel the cadence of words —Grace Fletcher⟩ ⟨his lyrics ~ and flow, with simple, fresh imagery, with delicacy and often humor —Eleanor Sickels⟩ **4 a :** to produce musical or harmonious sounds ⟨grasshoppers chirping and birds ~ing —G.B.Shaw⟩ ⟨frogs and crickets *sang* —Rex Ingamells⟩ ⟨most mysterious thing about a pack of hounds is the way they ~ or ... chime —Thurstan Holland-Hibbert⟩ **b :** to give forth such sounds when played ⟨when the violin *sang* —J.D.Carr⟩ ⟨to hear the heavy tuba ~ sweetly —Arthur Berger⟩ **5** *obs* **:** to chant or intone a religious observance ⟨sad and solemn priests still ~ for Richard's soul —Shak.⟩ **6 a :** to be filled with a humming or buzzing **:** RING ⟨next moment her ears were ~ing —Audrey Barker⟩ **b :** to be heard repetitively in the imagination **:** ECHO ⟨their murmured words of farewell *sang* in my ears —Eula Long⟩ ⟨voice saying, Remember my party, Remember my party, *sang* in his ears —Virginia Woolf⟩ **7 :** to be fit or apt for vocal rendition ⟨thinks *Medea* ~s as well as any concert work she knows —*Time*⟩ ⟨any translation would be something of a pity when it ~s so well in French —Douglas Watt⟩ **8 :** to make a cry **:** CALL — usu. used with *out* ⟨heard the captain of his escort ~ out to him in the darkness —Winston Churchill⟩ ⟨"You don't feel weak, or anything?" she *sung* out at me —Mary R. Rinehart⟩ **9 :** to give evidence or information ⟨is tough enough to have his goons dispatch anyone who dares to ~ to a crime commission —A.H.Weiler⟩ ⟨*sang* to a grand jury in return for a promise of leniency —*Time*⟩ ⟨don't let him know we *sung* on him —Priest Collins⟩ ~ *vt* **1 a :** to utter with musical inflections; *esp* **:** to interpret in musical tones produced by the voice ⟨~ a tune⟩ ⟨~ the tenor part⟩ **b :** to produce vocally the musical tones of ⟨~ G⟩ **2 a :** to relate, describe, or celebrate (something) in verse ⟨~*ing* the beauties of the garden and of simplicity —John Ciardi⟩ ⟨in antique style it ~s the loss of friends and fields —H.O.Taylor⟩ ⟨as men have loved their lovers ... and *sung* their wit, their virtue, and their grace —Edna S. V. Millay⟩ **b :** to announce or proclaim in a clear or resonant manner ⟨stationmaster ~*ing* the stops to the west coast⟩ — often used with *out* ⟨the bell ~*ing out* the hour of midnight⟩ **3 :** CHANT, INTONE ⟨a high mass of requiem ... will be *sung* —*N.Y.Times*⟩ **4 a :** to bring or accompany to a place or state by singing ⟨~s the child to sleep⟩ ⟨his blithe and cheerful verse *sang* itself into the memory —Brander Matthews⟩ **b :** to move or drive by singing ⟨hopes to ~ away his troubles⟩ — **sing one's praises :** to laud a person or thing vigorously and openly ⟨the west country thereafter is the richer for one more pen to *sing its praises* —*Times Lit. Supp.*⟩ ⟨parents *singing his praises* after the award⟩ — **sing the blues :** to express a pessimistic or discouraged attitude **:** COMPLAIN ⟨called me every now and then to *sing the blues* about her troubles —Polly Adler⟩

²**sing** \"\ *n* -s **:** the act of singing: as **a :** a singing esp. in company ⟨an all-night gospel ~ down South —Furman Bisher⟩ **b :** a ritualistic ceremony of a primitive society consisting largely of chanting ⟨without instruction the Navajo chorus at a ~ provides a moving choral performance —Joyce R. Muench⟩

sing *abbr* **1** single **2** singular **3** [L *singulorum*] of each

sing·able \ˈsiŋəbəl\ *adj* [ME *singabil* (part trans. of LL *cantabilis*) fr. *singen* to sing + L *-abilis* -able] **:** apt or suitable for singing ⟨every word is ~ and modestly poetic —Winthrop Sargeant⟩ ⟨agrees that ~ melody is the essence of music —Winthrop Sargeant⟩

singa·pore \ˈsiŋ(g)əˌpō(ə)r, -ō(ə)r, -ōə, -ō(ə) *also* ˌ≈≈ˈ≈\ *adj, usu cap* [fr. *Singapore*, Asia] **:** of or from the city or the country of Singapore **:** of the kind or style prevalent in Singapore

¹**singa·po·re·an** \ˌ≈≈ˈpōrēən, -pōr-\ *adj, usu cap* [*Singapore*, country and its capital off the south end of the Malay peninsula (fr. Malay *Singapora*, fr. Skt *Simhapura*, lit., lion city, fr. *simha* lion + *pura* city) + E *-an*] **1 :** of, relating to, or characteristic of Singapore, southeast Asia **2 :** of, relating to, or characteristic of the people of Singapore

²**singaporean** \"\ *n* -s *cap* **:** a native or resident of Singapore

singapore sling *n, usu cap 1st S* **:** a sling in which cherry brandy and sometimes Benedictine are added to the usual gin base

¹**singe** \ˈsinj\ *vt* **singed**; **singed**; **singeing**; **singes** [ME *sengen*, fr. OE *sengan*; akin to OHG *bisengan* to singe, OFris *ofsendza* to singe off, scorch, MD *sengen* to singe, MHG *senge* dryness, Sw dial. *sjängla* to singe, OSlav *isęčiti* to dry] **1 :** to burn (something) superficially or lightly **:** SCORCH: as **a :** to remove the hair or down from (an animal or fowl) by passing over a flame **b :** to remove projecting fibers and fuzz from (thread, yarn, or cloth) by passing rapidly over a gas flame or heated rollers **2 :** to cause (a person) unexpected trouble, distress, or embarrassment (as for an injudicious interference or venture) ⟨after being *singed* once or twice, I gave up on direct haggling —C.W.Morton⟩ **syn** see BURN

²**singe** \"\ *n* -s **:** a slight burn **:** SCORCH

³**singe** *obs var of* SIGN

singed \ˈsinjd\ *adj* [ME *senged*, fr. past part. of *sengen* to singe] **1 :** that has undergone singeing **2** *of fur* **:** having dried or curled over guard hairs caused by an animal's rubbing or inferior processing

singed cat *n* **:** one that is of better quality than appearance indicates ⟨had an instinctive sympathy for underpups and *singed cats* and the courage to champion their causes —I.S. Cobb⟩

¹**sing·er** \ˈsiŋə(r)\ *n* -s [ME, fr. *singen* to sing + *-er* — more at SING] **:** one that sings: as **a :** one whose profession is to sing **:** vocal artist **b :** POET ⟨the sweet ~ of Avon⟩ **c :** a bird with a natural or acquired ability to sing **:** SONGBIRD **d :** one of an order of officials managing and taking part in the psalmody in the early Christian church **e :** a primitive medicine man who cures sickness and gets rid of evil influences by means of a chanted ritual

²**sing·er** \ˈsinjə(r)\ *n* -s [¹*singe* + *-er*] **:** one that singes: as **a :** a textile worker who singes cloth **b :** one that singes surplus threads from shoe uppers with a gas flame or torch **c :** a slaughterhouse worker who removes hair from hog carcasses with a singeing torch

sin·ge·rie \(ˌ)saⁿzhˈrē, ˌsaⁿzhəˈrē\ *n* -s [F, fr. *singe* ape (fr. L *simius, simia*) + *-erie* -ery — more at SIMIAN] **:** a picture, decoration, or design in which monkeys are depicted

sing·er's node \ˈsiŋə(r)z-\ *n* **:** a thickening of tissue on a vocal cord resulting from excessive or incorrect use of the voice

singh \ˈsiŋ\ *n* -s [Hindi *siṅgh*, lit., lion, fr. Skt *siṁha*] **:** a member of one of the warrior castes of northern India; *specif* **:** a Sikh baptized into the Khalsa

singhalese *or* **singalese** *usu cap, var of* SINHALESE

singing *n* -s [ME, fr. gerund of *singen* to sing] **1 :** the act or sound of one that sings **2 :** SING a — often used in pl. ⟨Sunday night ~s for the young people —J.W.Frey⟩ **3 :** a whining, whistling, or humming sound made by something in vibration ⟨the ~ of crosscut saws —*Amer. Guide Series: Mich.*⟩ ⟨the strange high ~ of some aeroplane overhead —Virginia Woolf⟩; *specif* **:** a humming or ringing in one's ears

singing arc *n* **:** a direct current arc in parallel with which is a local circuit containing a condenser and inductance in series where oscillations take place according to the tuning and cause the arc to emit a musical note — compare POULSEN ARC

singing bird *n* **1 :** SONGBIRD **2 :** a passerine bird

singing canary *n* **:** BELUGA 2

singing falcon *or* **singing hawk** *n* **:** CHANTING FALCON

singing fish *n* **:** the midshipman (*Porichthys notatus*) or a related toadfish that makes a humming sound by vibration of the air bladder

singing flame *n* **:** MUSICAL FLAME

singing game *n* **1 :** a game (as *Farmer in the Dell* or *London Bridge*) in which the players accompany their actions with the singing of a narrative song **2 :** SWINGING PLAY

singing gibbon *n* **:** SILVER GIBBON

sing·ing·ly *adj* **:** in a singing manner **:** LYRICALLY

singing muscle *n* **:** an intrinsic syringeal muscle in a bird

sing·ka·mas *also* **sincamas** \ˌsēŋkäˈmäs\ *n* -ES [Tag, fr. MexSp *jícama*, fr. Nahuatl *xicama*] **:** YAM BEAN

¹**sin·gle** \ˈsiŋgəl\ *adj* [ME *single, sengle*, fr. MF, fr. L *singulus* one only, individual; akin to L *sem-* one — more at SAME] **1 a :** living in an unmarried state **:** CELIBATE ⟨take anything she can get in the way of a husband rather than face penury as a ~ woman —G.B.Shaw⟩ **b :** of or relating to celibacy ⟨prefers the ~ state⟩ **2 :** unattended or unaccompanied by others **:** SOLITARY ⟨he is left alone ~ and unsupported, like a leafless trunk —*Mirror*⟩ **3 a** (1) **:** consisting of or having only one part, feature, or portion as opposed to or contrasted with double or complex ⟨double consonants are often used in place of ~ consonants⟩ ⟨binocular ~ vision was tested —H.G. Armstrong⟩ (2) **:** consisting of one as opposed to or in contrast with many **:** UNIFORM ⟨undertaking to justify a ~ scale of rates for the entire country —W.M.W.Splawn⟩ ⟨the states sought a ~ type of automobile plate⟩ (3) **:** consisting of only one in number ⟨a ~ anchor holds the boat⟩ ⟨holds to a ~ ideal⟩ — often used with *not* ⟨not a ~ opponent of statehood appeared before the committee —*Midwest Jour.*⟩ ⟨has not made one ~ concession to any other quarter —R.T.H.Fletcher⟩ **b :** having only the normal number of petals or rays **:** not double — used esp. of a horticultural plant ⟨a ~ rose⟩ **4 a :** of or relating to a particular member or part **:** INDIVIDUAL ⟨when nature is so careless of the ~ life, why should we coddle ourselves —R.L.Stevenson⟩ ⟨each ~ citizen is an important part of the community⟩ **b :** of, relating to, or involving only one person ⟨check his ~ judgments against a larger conception or in a perspective of the whole —Meyer Schapiro⟩ ⟨will try his ~ strength against all the world⟩ **5 a** *obs* **:** lacking qualification or addition **:** PLAIN **b** *archaic* **:** of poor quality **:** WEAK ⟨drank his ~ ale⟩ **6 :** taken by itself apart from its group or constituency **:** DISTINCT, SEPARATE ⟨every ~ minute I kept wishing —Agnes S. Turnbull⟩ ⟨the most important ~ resource —B.B.Jennings⟩ ⟨more than any other ~ influence of their period —*Amer. Guide Series: Texas*⟩ ⟨the largest ~ agency providing assistance —Shlomo Katz⟩ **7 a :** free from duplicity or insincerity **:** FRANK, HONEST, OPEN ⟨the willingness of the incumbent ... to devote himself with a ~ mind to the public good —R.M.Dawson⟩ ⟨jealousy is the flaw in the ~ heart —Ellen Glasgow⟩ ⟨keep your eye ~ and your hands clean —Charles Kingsley⟩ **b :** exclusively concerned or attentive — usu. used of an eye ⟨lives with an eye ~ to his own advantage —*New Republic*⟩ ⟨everything in this line has been procured ... with an eye ~ to the taste of his numerous patrons —D.D.Martin⟩ **8 :** consisting of a whole **:** UNBROKEN, UNDIVIDED ⟨science and speed have made our world into a ~ neighborhood —Barbara Ward⟩ ⟨the great cause was the same; the source of all the movements was elemental, natural, and ~ —J.L.Motley⟩ **9 :** having one on each side **:** man to man ⟨who now defies thee thrice to ~ fight —John Milton⟩ **10 :** having no equal or like **:** UNUSUAL, SINGULAR ⟨was that rare critic, perhaps even that unique and ~ critic —J.C.Ransom⟩ ⟨~ among his fellows⟩ **11 :** ONLY, SOLE ⟨his ~ speech, that of January 31, 1861, received high praise —W.C.Ford⟩ ⟨his ~ intent was to speak a word of sympathy —A.T.Quiller-Couch⟩ ⟨the ~ piece of evidence⟩ **12 :** having the added musical part lying uniformly above or below the cantus firmus in two-part counterpoint **13 :** designed for the use of one person or family only ⟨a ~ room⟩ ⟨a ~ house⟩

syn SOLE, UNIQUE, LONE, SOLITARY, SEPARATE, PARTICULAR: SINGLE applies to that consisting of one alone and not capable of being felt as accompanied by or joined with another ⟨a *single* instance⟩ ⟨a *single* currency system⟩ ⟨Maine ... is the only one adjoined by but a single sister state —*Amer. Guide Series: Maine*⟩ ⟨the lover imagines but a *single* joy; to be master of his love in body and soul —George Santayana⟩ SOLE may intensify the notion that what is under consideration is the only one ⟨the *sole* lien to the estate⟩ ⟨the *sole* product of his factory⟩ ⟨invention is almost never the *sole* work of a single inventor —Lewis Mumford⟩ ⟨buy out his partners ... and thus become *sole* stockholder —*Current Biog.*⟩ ⟨the *sole* casualty of the battle ... was one cow —R.W.Hatch⟩ UNIQUE in reference to things like manuscripts and coins designates the only one extant; in other uses it indicates that which stands alone because of its unusual character ⟨the manuscript of Beowulf is *unique*⟩ ⟨the *unique* character of the English conquest of Britain needs special emphasis —Kemp Malone⟩ ⟨a *unique* combination of warm and relatively sunny winters, and a summer without excessively high temperatures —E.L.Ullman⟩ LONE and SOLITARY may suggest both single and isolated ⟨who in cells deep and *lone* have languished —P.B.Shelley⟩ ⟨the ambitious Aaron Burr who played a *lone* hand against the field —V.L.Parrington⟩ ⟨the *solitary* sin of an otherwise blameless character⟩ ⟨a sentry kept *solitary* vigil —J.H. Cutler⟩ SEPARATE stresses lack of connection with others; it indicates discreteness rather than singleness ⟨there was no *separate* church, in our sense of the term, as an independent organism within the state —G.L.Dickinson⟩ ⟨given in two *separate* and distinct sections of the constitution —John Marshall⟩ PARTICULAR in this sense stresses the fact of being regarded as distinct ⟨we shall venture beyond the *particular* book in search of qualities that group books together —Virginia Woolf⟩ ⟨some *particular* achievement of modern technology, like an electric shaver or the automobile —D.W. Brogan⟩

²**single** \"\ *n* -s [ME *sengle*, fr. *sengle*, adj., single] **1 a :** a claw of a hawk or falcon **b :** the tail of a deer **2 a :** a separate individual person ⟨the guests arrive in ~s and pairs⟩ **b :** a separate individual member of a large class of similar or identical objects: as (1) **:** a one-dollar bill ⟨flashing a big bankroll, generally a wad of ~s wrapped up in a hundred-dollar bill —*Police Gazette*⟩ (2) **:** a phonograph record usu. with not over five minutes of recording on each side ⟨will release the sides both as ~s and as an ... LP record —*Down Beat*⟩ (3) **:** a piece or section of sheet metal over 1/32 of an inch in thickness — used in pl. **c :** a modification of the coursing order in change ringing consisting of holding one bell in place through several changes **3 singles** *pl* **:** change ringing as performed on four bells **4 a :** a continuous strand of reeled or spun silk **b :** a thread or yarn of any fiber that is twisted or thrown — often used in pl. **5 a :** a hit for one run in the game of cricket **b :** ONE-BASE HIT **6 singles** *pl* **a :** a tennis match or similar game with one player on each side ⟨we play ~s or doubles⟩ **b :** a golf match between two players — distinguished from *foursome* **7 :** a boat or shell propelled by one oarsman **8 a :** a performance or entertainment by only one person ⟨offers to do ~s on other shows and in some clubs —*Newsweek*⟩ **b :** a person who does a single ⟨started hiring out as a ~ at lodge dances —*Time*⟩ **9 :** a flower having the normal number of petals or ray florets typical of the species **10 :** a room, apartment, or house designed to accommodate one person or one family ⟨the apartment is a ~⟩ ⟨small ~s of five and six rooms —Brendon Shea⟩

³**single** \"\ *vb* **singled**; **singled**; **singling** \-g(ə)liŋ\ **singles** [¹*single*] *vt* **1 a** *archaic* **:** to move asunder **:** PART, SEPARATE **b :** to separate (an animal) from a herd in order to chase or

hunt separately ⟨~ out a young cow⟩ **2** *obs* **:** to lead aside **:** SEQUESTER, WITHDRAW ⟨I have ~*ed* thee alone —Shak.⟩ **3 a :** to select or distinguish (a person or thing) from a number or group ⟨walks up to the line and ~s every 10th man⟩ — usu. used with *out* ⟨~s out for special praise the guidebook to Wells cathedral —Pyke Johnson⟩ **b :** to select or distinguish (a person or thing) for especial attention or comment — usu. used with *out* ⟨something about his person that *singled* him out from the rest of the punctual moving crowd —E.V. Lucas⟩ ⟨had *singled* him out as his successor —John Buchan⟩ ⟨all I can do is to ~ out a few of the basic ideas —A.W. Hummel⟩ **4** *Brit* **:** to thin (seedlings) so as to leave space between the plants **5 a** *archaic* **:** to reduce to only one **:** CONCENTRATE **b :** to reduce (as a doubled rope) from a number of parts to one **6 a :** to advance (a base runner) by a one-base hit ⟨*singled* him to third base⟩ **b :** to bring about the scoring of (a run) by a one-base hit ~ *vi* **1** *archaic* **:** to separate oneself from others **:** proceed alone **2 :** to thin out seedlings **3 :** to take in all bights of mooring lines on a ship except single lines preparatory to getting under way — usu. used with *up* **4 :** to make a one-base hit ⟨*singled* to center and knocked in two more runs —James Thurber⟩ ⟨*singled* behind his catcher —John Drebinger⟩

⁴single \"\ *adv* **:** SINGLY

single-acting \ˈ==ˈ==\ *adj* **:** acting in one direction only ⟨a *single-acting* plunger⟩

single-action \ˈ==ˈ=\ *adj* **1 :** SINGLE-ACTING **2** *of a firearm* **:** that requires cocking before each shot

single-banked \ˈ==ˈbaŋkt, -aiŋ-\ *adj* **:** having a single bank or row: as **a :** having a single row of oarsmen or one on each thwart with the oars alternating on each side **b :** having but one tier of oarsmen (as a unireme) — compare DOUBLE-BANKED

singlebar \ˈ==,=\ *n* [¹*single* + *bar*] **:** SINGLETREE

single-barrel \ˈ==ˈ==\ *n* **:** a single-barreled gun

single-barreled \ˈ==ˈbarəld *also* -ber-\ *adj*, *of a gun* **:** having one barrel

single-base powder \ˈ==ˈ=-\ *n* **:** an explosive powder or propellant that contains nitrocellulose as the only essential component — compare DOUBLE-BASE POWDER

single bill *or* **single bond** *n* **1 :** a bill or bond for the future payment of money with no annexed condition **2 :** a bill on which a single party is to be heard in a judicial proceeding

single bond *n* **:** SIMPLE BOND

single-breasted \ˈ==ˈ==\ *adj*, *of a coat or jacket* **:** having a center closing with one row of buttons and no lap — compare DOUBLE-BREASTED

single brilliant *n* **:** a brilliant with 16 facets above the girdle and 12 or 16 facets below

single-chamber \ˈ==ˈ==\ *adj* **:** having a single chamber **:** UNICAMERAL ⟨a *single-chamber* legislature⟩

single-coat·ed \ˈ==ˈkōd·əd\ *adj*, *of paper or board* **:** coated only once on one or both sides

single comb *n* **:** a comb on a fowl having the form of an erect or pendant median serrated crest — see COMB illustration

single corner *n* **:** one of the two diagonally opposed corners of a checkerboard that have a single dark or playing square

single counterpoint *n* **:** counterpoint in which the added part lies uniformly above or below the cantus firmus

single-crop \ˈ==ˈ=\ *vi* **:** to practice one-crop farming **:** grow a single crop on the same land repeatedly ~ *vt* **:** to use (land) in a one-crop system ⟨*single-cropping* their lands with wheat —*Rev. of Reviews*⟩

single cross *n* **:** the heterotic first generation hybrid between two selected and usu. inbred lines ⟨many commercial hybrid seeds are *single crosses*⟩ — compare DOUBLE CROSS, HETEROSIS, TOPCROSS

single cut *n* **:** a simplified brilliant cut used on small stones — see CUT illustration

single-cut file \ˈ==ˈ=-\ *n* **:** a file having a single parallel series of diagonal cuts across its face

single doubler *n* **:** DOUBLER 2a

single-end·ed \ˈ==ˈendəd\ *adj* **:** having the principal or working portion at one end only ⟨a *single-ended* boiler⟩

single entry *n* **:** a method or system of bookkeeping that recognizes only one side of a business transaction and usu. consists only of a record of cash and personal accounts with debtors and creditors — compare DOUBLE ENTRY

single-entry table *n* **:** a mathematical table in which a tabulated function depends on but one independent variable

single escheat *n*, *Scots law* **:** escheat to the crown of one's movable estate

single-eye \ˈ==ˈ=\ *adj* **:** having only one bud ⟨a *single-eye* cutting⟩

single-eyed \ˈ==ˈ=\ *adj* **1 :** having a clear honest eye **:** SINGLE **2 :** having but one eye or the sight of one eye

¹single file *n* **:** a line of persons, animals, or things moving one behind another; *also* **:** a single row — called also *Indian file* ⟨marching in *single file*⟩

²single file *adv* **:** in a single line ⟨traffic is slowed by having to crawl *single file* through the doors in the . . . barricades —Mollie Panter-Downes⟩

single-file \ˈ==ˈ=\ *vi* [fr. *single file*, n.] **:** to walk or move in single file ⟨all *single-filed* past the . . . bed —J.D.Salinger⟩ ⟨*single-filing* down the St. George's channel to Liverpool —Gordon Webber⟩

single fish *n* **:** a single fish joint

¹single-foot \ˈ==,=\ *n*, *pl* **single-foots :** ⁷RACK b

²single-foot \"\ *vi*, *of a horse* **:** to go at a rack ⟨has seen him *single-foot* up to a wall and go over clear —Allan Forbes & R.M.Eastman⟩ — **single-footer** \ˈ==,==\ *n*

single-framed roof \ˈ==ˈ=-\ *n* **:** a roof in which opposite rafters are tied together by the upper floor frame or by boards nailed across horizontally

single-gear \ˈ==ˈ=\ *vt* **:** to gear directly (as by belting or a single pair or train of gear wheels) without the use of any additional speed-reducing mechanism

¹single-handed \ˈ==ˈ==\ *also* **single-hand** \ˈ==ˈ=\ *adj* **1 :** managed or done by one person or with one on a side ⟨account of his *single-handed* journeys in the sixties —*Brit. Bk. News*⟩ ⟨a cannon used . . . in his *single-handed* defense of the local coastline —*Amer. Guide Series: Conn.*⟩ ⟨fighting in *single-handed* combat⟩ **2 :** working alone or unassisted by others ⟨reference book . . . for the *single-handed* cook with a family to feed —Margaret Lane⟩ ⟨people who are *single-handed* or too old to manage holdings —A.D.Rees⟩ **3 :** used or adapted for using with one hand ⟨*single-handed* fishing rod⟩ **4 :** having or using only one hand ⟨a *single-handed* billiard player⟩ — **single-hand·ed·ness** *n* -ES

²single-handed \"\ *adv* **:** with or by oneself or without assistance ⟨fought his own cause in both war and politics *single-handed* —*advt*⟩ ⟨had to build his little log hut *single-handed* —A.F.Harlow⟩

single-hand·ed·ly *adv* **:** in a single-handed manner ⟨undertook the superhuman task of *single-handedly* creating a historical dictionary —Robert Pick⟩

single-hearted \ˈ==ˈ==\ *adj* **1 :** SINGLE 7a ⟨the perfect, *single-hearted*, crusading knight —H.O.Taylor⟩ **2 :** characterized by or resulting from sincerity and unity of purpose or dedication ⟨such a task requires an expenditure of time and energy, a *single-hearted* consecration —B.N.Cardozo⟩ ⟨the man who seizes on one deep-reaching idea . . . and with *single-hearted* fervor forces it upon the world —P.E.More⟩ ⟨her lifelong, *single-hearted*, and unshakable conviction —Albert Lynd⟩

single-heart·ed·ly *adv* **:** in a single-hearted manner ⟨works nobly and *single-heartedly*⟩

single-heart·ed·ness *n* -ES **:** the quality or state of being single-hearted ⟨fervent saint who sang because he suffered, and whose mysticism was tinged with kindly *single-heartedness* —Frances P. Keyes⟩

single jack *n* **:** a short-handled hammer weighing about four pounds and used in hand drilling

single jacker *n* **:** a miner using a single jack

single knot *n* **:** OVERHAND KNOT

single-leaf \ˈ==,=\ *or* **single-leaf pine** *or* **single-leaf pinyon** *n* **:** PIÑON

single-leaf ash *also* **single-leaved ash** *n* **:** a unifoliolate or rarely bifoliolate or trifoliolate ash (*Fraxinus anomala*) of the western U.S.

single-line \ˈ==ˈ=\ *adj* **:** confining commercial activity to one line of goods ⟨a *single-line* manufacturer⟩ ⟨a *single-line* representative⟩

single-loader \ˈ==ˈlōdə(r)\ *n* **:** a firearm in which each charge is inserted separately

single man *n* **:** a checker that may be moved only forward — compare KING

single-member district \ˈ==ˈ==-\ *also* **single-member constituency** *n* **:** an electoral district or constituency having a single representative in a legislative body rather than two or more — compare LIST SYSTEM, PROPORTIONAL REPRESENTATION

single-minded \ˈ==ˈ==\ *adj* **1 :** SINGLE 7a ⟨a dedicated, *single-minded* man —*Time*⟩ ⟨an honest, farsighted, *single-minded* and liberal statesman —J.F.Gore⟩ — opposed to *double-minded* **2 :** SINGLE-HEARTED 2 ⟨his *single-minded*, selfless devotion to the liberation of his country —H.H. Fisher⟩ ⟨had a *single-minded* love of God and a catholic love of humanity —W.L.Sperry⟩ **3 :** having one unifying purpose ⟨with all the emotional ferocity and energy of genius, was *single-minded* for victory —J.H.Plumb⟩ ⟨his *single-minded* concern with the political dimension —Martin Price⟩ ⟨affable manner covered a *single-minded* ruthlessness —*Time*⟩

single-mind·ed·ly *adv* **:** in a single-minded manner

single-mind·ed·ness *n* -ES **:** the quality or state of being single-minded ⟨had a passionate *single-mindedness* which their divided minds and loyalties lacked —W.L.Sperry⟩

single money *n*, *obs* **:** small currency **:** SMALL CHANGE

single-name paper \ˈ==ˈ=-\ *n* **:** a promissory note with no endorsement other than the signature of the maker

sin·gle·ness *n* -ES [¹*single* + *-ness*] **1 :** sincerity and honesty in design or intent **:** STRAIGHTFORWARDNESS ⟨a man the ~ of whose motives could not be questioned —Winston Churchill⟩ ⟨those who with ~ of mind try to do God's will —*Interpreter's Bible*⟩ **2 :** the state of being unmarried **:** CELIBACY ⟨traces the trends in nuptiality and ~ —*Population Index*⟩ **3 :** the fact of being single or one of a kind or group **:** ONENESS ⟨the ~ of a small operation . . . lost in the confusion of dozens of outfits —H.D.Skidmore⟩ **4 :** the condition of standing or remaining alone or apart ⟨the vulnerability of ~ will disappear before unity of effort —Douglas MacArthur⟩ **5 :** the quality of concentrating on one central objective ⟨the ~ of our aim generates a tremendous sense of solidarity —F.A. Perry⟩

single nickel salt *n* **:** NICKEL SULFATE

single-nose \ˈ==ˈ=\ *adj* **:** having only one growing point and usu. producing a single flower stalk ⟨a *single-nose* narcissus bulb⟩ — compare DOUBLE-NOSE

single-pass \ˈ==ˈ=\ *vt* **:** to pass (gases) once across the tubes of a boiler

single-phase \ˈ==ˈ=\ *adj* **:** of or relating to a circuit energized by a single alternating electromotive force with the currents in the two wires differing in phase by 180 degrees or a half cycle

single-phaser \ˈ==ˈ==\ *n* **:** a single-phase machine

single-phasing \ˈ==ˈ==\ *n* -s **:** the operation of a polyphase motor on single-phase supply

single-pole switch \ˈ==ˈ=-\ *n* **:** an electric switch having only one blade and one contact

single premium *n* **:** the sum that would meet in a single payment the cost of a life insurance policy for the entire policy term

single-punch \ˈ==ˈ=\ *vt* **:** to punch one hole at a time in

single-rail crane \ˈ==ˈ=-\ *n* **:** WALKING CRANE

single-rail track circuit *n* **:** a track circuit comprising two running rails with one divided into sections by insulated joints and the other used as a common return

single rhyme *n* **:** a monosyllabic rhyme

single-rivet \ˈ==ˈ==\ *vt* **:** to secure (a joint) by a single row of rivets or by a single row on each side of the seam of a butt joint

singles *pl of* SINGLE, *pres 3d sing of* SINGLE

singles court *n* **:** a court (as for tennis) laid out for only two players

single-screw \ˈ==ˈ=\ *adj* **:** having one screw propeller ⟨a *single-screw* ship⟩ — compare TWIN-SCREW

single-seater \ˈ==ˈ==\ *n* **:** a vehicle (as an airplane) with a single seat

single-seed cucumber \ˈ==ˈ=-\ *n* **:** STAR CUCUMBER

single shear *n* **:** shear along one surface only

single-shear steel *n* **:** SHEAR STEEL

single-shot \ˈ==ˈ=\ *adj* **:** capable of firing only one shot without reloading

single-shot pistol *n* **:** a pistol that can be loaded with only one cartridge at a time and that is used chiefly in target practice — compare AUTOMATIC PISTOL

single-side-band modulation \ˈ==ˈ=,=-\ *n* **:** a modulation used in a radio or telephone carrier in which the normal carrier signal is eliminated and one of the two modulation side bands is removed usu. by filtering

single-side-band transmission *n* **:** carrier suppression in which the power associated essentially with one side band is not transmitted

single-space \ˈ==ˈ=\ *vt* **:** to type (copy) leaving no blank line spaces ⟨*single-space* the list of services, but leave a double space both before and after —D.D.Lessenberry & T.J.Crawford⟩ ~ *vi* **:** to type on every line space

single spanish burton *n*, *usu cap 2d S* **:** a tackle with three single blocks

single spruce *n* **:** WHITE SPRUCE 1a

single-stage \ˈ==ˈ=\ *adj* **:** of one stage only **:** complete in one rather than in two or more operations ⟨*single-stage* turbine⟩ ⟨*single-stage* rocket⟩ ⟨*single-stage* trigger⟩

single standard *n* **1 :** MONOMETALLISM **2 :** a set of principles that apply equally to all members of a group; *specif* **:** a code of morals that applies the same standards of sexual behavior to both men and women — compare DOUBLE STANDARD

singlestick \ˈ==,=\ *n* [¹*single* + *stick*] **1 :** fighting or fencing with a one-handed wooden stick or sword ⟨the crisp click of sportsmen at ~ —Lawrence Durrell⟩ **2 :** the weapon used in singlestick combat

singlesticker \ˈ==,==\ *n* [¹*single* + *stick* + *-er*] **:** a single-masted vessel **:** SLOOP, CUTTER

single stitch *n* **:** a bookbinder's stitch made by passing a single loop through the center of the matter to be secured and tying

single-surfaced \ˈ==ˈ==\ *adj* **:** having one finished surface ⟨*single-surfaced* airplane wing⟩

sin·glet \ˈsiŋglət, *usu* -əd·+V\ *n* -s [¹*single* + *-et*] **1 a** *dial chiefly Brit* **:** an unlined waistcoat **b** *chiefly Brit* **:** an undershirt or athletic jersey ⟨his coppery-brown torso that was only partly covered by the torn ~ —Vance Palmer⟩ ⟨athletes, stripped to their ~s and shorts, raced, cycled and pole-jumped —H.V.Morton⟩ **2 a :** an atomic, molecular, or nuclear energy level with a spin of zero **b :** a spectrum line that is not resolved into components by even the highest dispersion

single-tap r \ˈ==ˈ=-\ *n* **:** a trilled *r* made by a single flip of the point of the tongue against the teethridge (as in the southern British pronunciation of *very* sometimes spelled *veddy*)

sin·gle·tary pea \ˈsiŋgəl,terē-\ *n* [*singletary* prob. fr. ¹*single* + *-tary* (as in *solitary*); fr. its being an escape] **:** a weak-stemmed and usu. decumbent winter annual legume (*Lathyrus hirsutus*) native to the Mediterranean region but long established as an escape in the southern U.S. and more recently cultivated as a cover and pasture crop — called also *Caley pea, rough pea, wild winterpea*

single tax *n* **:** a tax to be levied on a single object as the sole source of public revenue esp. by taking the entire economic rent of land

single taxer *n* **:** an advocate of a single-tax system

single-throw switch \ˈ==ˈ=-\ *n* **:** a switch (as on an electrical switchboard) that by one operation engages a set of fixed contacts

sin·gle·ton \ˈsiŋgəltən, -tᵊn\ *n* -s [F, fr. E ¹*single* + F *-eton* (dim. suffix)] **1 :** a card (as in bridge) that is the only one of its suit orig. held in a hand — compare DOUBLETON **2 :** an individual member or thing distinct from others grouped with it ⟨a quatrain consisting of a triplet and a ~⟩ ⟨the birds scattered . . . and the ~s were easy to pick up one by one —Thomas Barbour⟩; *specif* **:** a single offspring ⟨in May or June the spotted fawns are born, usually ~s, but rarely twins —W.A.Weber⟩

single-tongue \ˈ==ˈ=\ *vi* [⁴*single* + *tongue*, v.] **:** to articulate notes on a wind instrument by repeated single articulations (as *t*, *t*) — compare DOUBLE-TONGUE

single-track \ˈ==ˈ=\ *adj* **1 :** having but one track ⟨a *single-track* railroad⟩ **2 :** lacking intellectual range, receptiveness, or flexibility **:** ONE-TRACK ⟨with a *single-track* mind devoted solely to his duty —Leo Crane⟩

single transferable vote *n* **:** a vote on a ballot that can be transferred from a candidate of first choice who has already obtained the necessary quota of votes for election to a candidate marked by the voter as second or third choice in order that every vote may count toward the election of a candidate — compare HARE SYSTEM

sin·gle·tree \ˈsiŋgəl·(ˌ)trē, -l·tri\ *n* [¹*single* + *tree*] **1 :** WHIFFLETREE **2 :** a heavy horizontal bar sometimes used to spread the loop of a hoisting chain to prevent crushing the load

single-valued \ˈ==ˈ=(ˌ)=\ *adj* **:** having only one value for any one value of the argument ⟨a *single-valued* function⟩

single vote *or* **single nontransferable vote** *n* **:** a simple form of proportional representation by which each voter casts his ballot for one candidate only

single whip *n* **:** a purchase consisting of a single block and a small rope for lifting light articles — compare DOUBLE WHIP

single wicket *n* **:** a variation of cricket that is played on a pitch with a single batting end having three stumps and a bowling end usu. marked by one stump with all bowling being done from the same end and but one batsman being in at a time

single wingback formation *or* **single wing** *n* **:** an offensive football formation to the left or right in which a back plays just outside of and a yard behind one of the ends, the blocking back is on the same side of the center and usu. a yard behind the guard, and the two other backs are four or five yards behind a balanced or unbalanced line and in a position to receive a direct snap from the center

singling *n* -s [fr. gerund of ³*single*] **1 :** the act or process of one that singles **2 singlings** *pl* **:** the crude product that first passes over in distilling **:** the low wine that is usu. redistilled at a lower temperature **3 :** a defect in the plying of yarns caused by the omission of one or more strands

sin·gly \ˈsiŋ(g)(ə)lē, -li\ *adv* [ME *sengely*, fr. *sengle* single + *-ly* — more at SINGLE] **1 a :** by or with oneself **:** as an individual person or thing **:** SEPARATELY ⟨they come ~ or in scattered groups —*Amer. Guide Series: Pa.*⟩ ⟨the tree-living primate mother and her ~ born infant —Weston La Barre⟩ **b :** without the assistance or support of others **:** SINGLE-HANDEDLY ⟨either ~ or in cooperation, have carried on noteworthy educational activities —*Amer. Guide Series: Oregon*⟩ ⟨~ and successfully opposed the . . . proposal for a drastic shortening of hours in industry —*Current Biog.*⟩ **2** *archaic* **:** as or by a single unit **:** EXCLUSIVELY, SOLELY **3 :** STRAIGHTFORWARDLY, HONESTLY, SINCERELY ⟨having its accomplishment ~ in mind —F.J.Haskin⟩

sing·pho \ˈsiŋ,pō\ *n*, *pl* **singpho** *or* **singphos** *usu cap* **:** CHINGPAW

sings *pres 3d sing of* SING, *pl of* SING

¹sing-sing \ˈsiŋ,siŋ\ *n* -s [Malinke *si-nsing* antelope] **:** a West African waterbuck (*Kobus defassa unctuosus*) distinguished by rather long sandy brown distinctly greasy hair

²sing-sing \"\ *n* [redupl. of ¹*sing*] **:** an Oceanian ceremony of singing and dancing

¹singsong \ˈ=,=\ *n* [¹*sing* + *song*] **1 a :** a verse selection with marked and regular rhythm and rhyme **:** a jingling song or ballad **b :** verse of such characteristics ⟨the ~ of the epic, its repetitious phrases and familiar story —*College English*⟩ **2** *chiefly Brit* **:** SING 1a ⟨food, refreshments, entertainment, and a ~ combined to make it a highly enjoyable evening —*Crowsnest*⟩ **3 :** a voice delivery characterized by a narrow range of pitch or a mechanically repetitious pitch variation ⟨began in the ~ of a professional guide —Donn Byrne⟩ ⟨the ~ of . . . campaign oratory —Max Ascoli⟩ ⟨the auctioneer with his rapid ~ —*Amer. Guide Series: Tenn.*⟩ ⟨speaking English in a Welsh ~ —John Barkham⟩

²singsong \"\ *adj* **1 :** making or delivering singsong ⟨is known as a ~ poet⟩ **2 :** characterized by the light or trivial usu. monotonously expressed ⟨writes ~ verse⟩ ⟨cases of long-windedness, foggy meanings, clichés, and ~ phrases —Stuart Chase⟩ **3 :** having a *monotonous* cadence or rhythm **:** marked by a singsong ⟨story in a deliberately rhythmical, ~ prose —*New Yorker*⟩ ⟨cultivated a ~ manner of speaking —Thomas Pyles⟩ ⟨the ~ orchestration from a loud radio sawed the air —Kathryn Grondahl⟩

³singsong \"\ *vb* -ED/-ING/-S *vt* **1 :** to move by *or as if* by means of a singsong or chant ⟨watched coolies ~ a dismantled truck up the cliff —*Time*⟩ **2 :** to speak, chant, or declaim in singsong ⟨the class ~*ing* the number tables⟩ ⟨~*ed* her way through Shakespeare with a . . . native-born inflection —Joan Comay⟩ ~ *vi* **:** to speak, chant, or sing in a singsong manner ⟨droning on and on, his voice ~*ing* almost unrecognizably —Norman Mailer⟩ ⟨vendors ~*ed* up and down the platform —Jobo Nakamura⟩

singsong girl *n* **:** a Chinese girl engaged in professional entertainment similar to that performed by the geisha

sing·songy \ˈ=,sȯŋē, -ŋi *also* -,säŋ-\ *adj* [¹*singsong* + *-y*] **:** suggestive of singsong

sing·spiel \ˈsiŋ,spēl, ˈziŋ,shpēl\ *n*, *usu cap* [G, fr. *singen* to sing (fr. OHG *singan*) + *spiel* play, fr. OHG *spil* — more at SING, SPIEL] **:** a somewhat dramatic musical work popular in Germany esp. in the latter part of the 18th century, usu. comic in nature, and characterized by spoken dialogue interspersed with popular or folk songs — compare BALLAD OPERA

sing·spi·ra·tion \ˌsiŋspəˈrāshən\ *n* -s [¹*sing* + *inspiration*] **:** a song service featuring the group singing of hymns conducted esp. by revivalistic churches and often followed by a sermon

¹sin·gu·lar \ˈsiŋgyələ(r)\ *adj* [ME *singuler*, fr. MF *singuler*, *singulier*, fr. L *singularis* single, solitary, singular, fr. *singulus* one only, individual + *-aris* -ar — more at SINGLE] **1 a :** of or relating to a separate person or thing **:** INDIVIDUAL ⟨every fact in the world might be ~, that is, unlike any other fact and sole of its kind —William James⟩ ⟨assumption that the ~ person can be understood apart from his culture —*Amer. Polit. Sci. Rev.*⟩ ⟨saw that each weed was a ~ knife —Stephen Crane⟩ ⟨to all and ~ to whom these presents shall come, greetings⟩ **b :** of, relating to, or being a word form denoting one person, thing, or instance ⟨one subject usually takes a ~ verb⟩ — opposed to *plural*; compare DUAL **c :** of or relating to a single instance or to something considered by itself **:** applied to only one individual ⟨a ~ term⟩ ⟨a ~ proposition⟩ — opposed to *general* **d** (1) **:** of or relating to a single or individual unit ⟨convey several parcels of land all and ~⟩ (2) **:** of, relating to, or affecting a particular property or one or more separate interests or rights in property as distinguished from the entire body of a decedent's estate or any interest or right in property acquired otherwise than by inheritance — compare SINGULAR SUCCESSION **2 a** *obs* **:** set apart or distinguished by superiority **:** EMINENT **b :** of considerable extent or worth **:** EXTRAORDINARY, EXCEPTIONAL ⟨achieved a ~ mechanical triumph that won him wide renown —Sherwood Anderson⟩ ⟨a ~ poetic achievement —H. W.V.Lange⟩ ⟨holds a ~ regard for his people⟩ ⟨his death is a ~ loss⟩ **c** *obs* **:** especially helpful or efficacious **:** BENEFICIAL **3** *archaic* **a :** consisting of one only **b :** having but one on each side ⟨those in his high place fight no ~ combats —Sir Walter Scott⟩ **4 a :** of unusual quality **:** UNCOMMON, UNIQUE ⟨various speculations put forward in explanation of the ~ phenomena of this remarkable place —Harry Luke⟩ ⟨a work of ~ originality and analytical power —*Economica*⟩ ⟨that woman of ~ mystery, the Mona Lisa —Elizabeth Janeway⟩ **b :** RARE, VALUABLE ⟨a man of ~ charm and sterling character —D.S. Muzzey⟩ ⟨an effect of ~ grace and delicacy —*Amer. Guide Series: Maine*⟩ ⟨of ~ and exquisite workmanship⟩ **5 a :** being at variance with others **:** DIFFERING, CONTRARY ⟨am not ~ in the opinion that much of the disease which does prevail might be avoided —Charles Dickens⟩ ⟨nor are we ~ in our judgment —Aldous Huxley⟩ **b :** departing from general usage or expectation **:** PECULIAR, ECCENTRIC ⟨a ~

EXHIBIT E-4

'S

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limp–wrist·ed \(ˈ)lim-ˈpris-təd\ *adj* (1966) **1 :** EFFEMINATE **2 :** WEAK
lim·u·lus \ˈlim-yə-ləs\ *n, pl* **-li** \-ˌlī, -ˌlē\ [NL, genus name, fr. L *limus* sidelong] (1837) **:** HORSESHOE CRAB
limy \ˈlī-mē\ *adj* **lim·i·er; -est** (ca. 1552) **1 :** smeared with or consisting of lime **:** VISCOUS **2 :** containing lime or limestone **3 :** resembling or having the qualities of lime
lin·ac \ˈlin-ˌak\ *n* (1950) **:** LINEAR ACCELERATOR
lin·age \ˈlī-nij\ *n* (1884) **:** the number of lines of printed or written matter
lin·alo·ol \lə-ˈnal-ə-ˌwȯl, lī-, -ˌwōl\ *n* [ISV, fr. MexSp *lináloe,* tree yielding perfume, fr. ML *lignum aloes,* lit., wood of the aloe] (1891) **:** a fragrant liquid alcohol $C_{10}H_{18}O$ that occurs both free and in the form of esters in many essential oils and is used in perfumes, soaps, and flavoring materials
linch·pin \ˈlinch-ˌpin\ *n* [ME *lynspin,* fr. *lyns* linchpin (fr. OE *lynis*) + *pin;* akin to OE *eln* ell] (13c) **1 :** a locking pin inserted crosswise (as through the end of an axle or shaft) **2 :** one that serves to hold together the elements of a complex ⟨the ~ in the prosecution's case was a subpoenaed canceled check —Joel Sayre⟩
Lin·coln \ˈliŋ-kən\ *n* [*Lincoln*shire, England] (1837) **:** any of an English breed of long-wool mutton-type sheep
Lin·coln·i·a·na \(ˌ)liŋ-ˌkō-nē-ˈan-ə, -ˈän-ə, -ˈā-nə\ *n pl* (1921) **:** materials relating to Abraham Lincoln
Lincoln's Birthday \ˌliŋ-kənz-\ *n* (1898) **1 :** February 12 observed as a legal holiday in many states of the U.S. **2 :** the first Monday in February observed as a legal holiday by some states of the U.S.
lin·co·my·cin \ˌliŋ-kə-ˈmīs-ᵊn\ *n* [*linco-* (fr. *Streptomyces lincolnensis*) + *-mycin*] (1963) **:** an antibiotic obtained from an actinomycete (*Streptomyces lincolnensis*) and effective esp. against cocci
lin·dane \ˈlin-ˌdān\ *n* [T. van der *Linden,* 20th cent. Du. chemist] (ca. 1949) **:** an insecticide that consists chiefly of the gamma isomer of BHC and is biodegraded very slowly
lin·den \ˈlin-dən\ *n* [ME, made of linden wood, fr. OE, fr. *lind* linden tree; prob. akin to OE *lithe* gentle — more at LITHE] (bef. 12c) **1 :** any of a genus (*Tilia* of the family Tiliaceae, the linden family) of trees that are native in temperate regions, are planted as shade trees, and are distinguished by having cordate leaves and a winglike bract attached to the peduncle of the flower and fruit: as **a :** a European tree (*T. europaea*) much used for ornamental planting **b :** a tall No. American forest tree (*T. americana*) — called also *basswood, whitewood* **2 :** the light fine-grained white wood of a linden; *esp* **:** BASSWOOD
lin·dy \ˈlin-dē\ *n* [prob. fr. *Lindy,* nickname of Charles A. Lindbergh] (1931) **:** a jitterbug dance originating in Harlem and later developing many local variants
[1]**line** \ˈlīn\ *vt* **lined; lin·ing** [ME *linen,* fr. *line* flax, fr. OE *līn* — more at LINEN] (bef. 12c) **1 :** to cover the inner surface of ⟨~ a cloak with silk⟩ **2 :** to put something in the inside of **:** FILL **3 :** to serve as the lining of ⟨tapestries *lined* the walls⟩ **4** *obs* **:** FORTIFY — **line one's pockets :** to take money freely and esp. dishonestly
[2]**line** *n, often attrib* [ME; partly fr. OF *ligne,* fr. L *linea,* fr. fem. of *lineus* made of flax, fr. *linum* flax; partly fr. OE *line;* akin to OE *līn*] (bef. 12c) **1 a :** THREAD, STRING, CORD, ROPE: as **(1) :** a comparatively strong slender cord **(2) :** CLOTHESLINE **(3) :** a rope used on shipboard **b (1) :** a device for catching fish consisting of a cord with hooks and other fishing gear **(2) :** scope for activity **c :** a length of material used in measuring and leveling **d :** piping for conveying a fluid (as steam) **e (1) :** a wire or pair of wires connecting one telegraph or telephone station with another or a whole system of such wires; *also* **:** any circuit in an electronic communication system **(2) :** a telephone connection ⟨tried to get a ~⟩; *also* **:** an individual telephone extension ⟨a call on ~ 2⟩ **(3) :** the principal circuits of an electric power system **2 a :** a horizontal row of written or printed characters; *also* **:** any of the successive horizontal rows of elements that constitute a television picture **b :** a unit in the rhythmic structure of verse formed by the grouping of a number of the smallest units of the rhythm (as metrical feet) **c :** a short letter **:** NOTE **d** *pl* **:** a certificate of marriage **e :** the words making up a part in a drama — usu. used in pl. **3 a :** something (as a ridge or seam) that is distinct, elongated, and narrow **b :** a narrow crease (as on the face) **:** WRINKLE **c :** the course or direction of something in motion **:** ROUTE **d (1) :** a state of agreement or conformity **:** ACCORDANCE **(2) :** a state of order, control, or obedience **e :** a boundary of an area ⟨the state ~⟩ **f :** the track and roadbed of a railway **4 a :** a course of conduct, action, or thought **b :** a field of activity or interest **c :** a glib often persuasive way of talking **5 a :** LIMIT, RESTRAINT **b** *archaic* **:** position in life **:** LOT **6 a (1) :** FAMILY, LINEAGE **(2) :** a strain produced and maintained by selective breeding **(3) :** a chronological series **b :** dispositions made to cover extended military positions and presenting a front to the enemy — usu. used in pl. **c :** a military formation in which the different elements are abreast of each other **d :** naval ships arranged in a regular order **e (1) :** the combatant forces of an army distinguished from the staff corps and supply services **(2) :** the force of a regular navy **f (1) :** officers of the navy eligible for command at sea distinguished from officers of the staff **(2) :** officers of the army belonging to a combatant branch **g :** an arrangement or placement of persons or objects of one kind in an orderly series ⟨a ~ of trees⟩ ⟨waiting in ~⟩; *also* **:** the persons or objects so positioned ⟨the ~ moved slowly at the bank⟩ **h (1) :** a group of public conveyances plying regularly under one management over a route **(2) :** a system of transportation together with its equipment, routes, and appurtenances; *also* **:** the company owning or operating it **i :** a succession of musical notes esp. considered in melodic phrases **j (1) :** an arrangement of operations in manufacturing permitting sequential occurrence on various stages of production **(2) :** the personnel of an organization that are responsible for its stated objective **k (1) :** the 7 players including center, 2 guards, 2 tackles, and 2 ends who in offensive football play line up on or within one foot of the line of scrimmage **(2) :** the players who in defensive play line up within one yard of the line of scrimmage **7 :** a narrow elongated mark drawn or projected: as **a (1) :** a circle of latitude or longitude on a map **(2) :** EQUATOR **b :** a mark (as on a map) recording a boundary, division, or contour **c :** any of the horizontal parallel strokes on a music staff on or between which notes are placed — compare SPACE **d :** a mark (as by pencil) that forms part of the formal design of a picture distinguished from the shading or color **e :** a division on a bridge score dividing the score for bonuses from that for tricks **f (1) :** a demarcation of a limit with reference to which the playing of some game or sport is regulated — usu. used in combination **(2) :** a marked or imaginary line across a playing area (as a football field) parallel to the end line **(3) :** LINE OF SCRIMMAGE **8 :** a straight or curved geometric element that is generated by a moving point and that has extension only along the path of the point **:** CURVE **9 a :** a defining outline **:** CONTOUR **b :** a general plan **:** MODEL — usu. used in pl. **10 a** *chiefly Brit* **:** PICA — used to indicate the size of large type **b :** the unit of fineness of halftones expressed as the number of screen lines to the linear inch **11 :** merchandise or services of the same general class for sale or regularly available **12 :** a source of information **:** INSIGHT **13 :** a complete game of 10 frames in bowling — called also *string* **14 :** LINE DRIVE — **liny** *also* **lin·ey** \ˈlī-nē\ *adj* — **between the lines 1 :** by implication **:** in an indirect way **2 :** by way of inference — **down the line :** all the way **:** FULLY — **in line for :** due or in a position to receive — **on line :** in or into operation — **on the line 1 :** in complete commitment and at great risk ⟨puts his future *on the line* by backing that policy⟩ **2 :** on the border between two categories **3 :** IMMEDIATELY ⟨paid cash *on the line*⟩
[3]**line** *vb* **lined; lin·ing** *vt* (1530) **1 :** to mark or cover with a line or lines **2 :** to depict with lines **:** DRAW **3 :** to place or form a line along ⟨pedestrians ~ the walks⟩ **4 :** to form into a line or lines **:** ALIGN ⟨~ up troops⟩ **5 :** to hit (as a baseball) hard and in a usu. straight line ~ *vi* **1 :** to hit a line drive in baseball **2 :** to come into the correct relative position **:** ALIGN
[1]**lin·eage** \ˈlin-ē-ij *also* ˈlin-ij\ *n* (14c) **1 a :** descent in a line from a common progenitor **b :** DERIVATION **2 :** a group of individuals tracing descent from a common ancestor; *esp* **:** such a group of persons whose common ancestor is regarded as its founder
[2]**line·age** \ˈlī-nij\ *var of* LINAGE
lin·eal \ˈlin-ē-əl\ *adj* (14c) **1 :** LINEAR **2 :** composed of or arranged in lines **3 a :** consisting of or being in a direct male or female line of ancestry **b :** relating to or derived from ancestors **:** HEREDITARY **c :** descended in a direct line **4 a :** belonging to one lineage ⟨~ relatives⟩ **b :** of, relating to, or dealing with a lineage — **lin·eal·i·ty** \ˌlin-ē-ˈal-ət-ē\ *n* — **lin·eal·ly** \ˈlin-ē-ə-lē\ *adv*
lin·ea·ment \ˈlin-ē-ə-mənt\ *n* [ME, fr. L *lineamentum,* fr. *linea*] (15c) **1 a :** an outline, feature, or contour of a body or figure and esp. of a face — usu. used in pl. **b :** a linear topographic feature (as of the earth or a planet) that reveals a characteristic (as a fault or the subsurface structure) **2 :** a distinguishing or characteristic feature — usu. used in pl. — **lin·ea·men·tal** \ˌlin-ē-ə-ˈment-ᵊl\ *adj*
lin·ear \ˈlin-ē-ər\ *adj* (1706) **1 a (1) :** of, relating to, resembling, or having a graph that is a line and esp. a straight line **:** STRAIGHT **(2) :** involving a single dimension **b (1) :** of the first degree with respect to one or more variables **(2) :** of, relating to, based on, or being linear equations, linear differential equations, linear functions, linear transformations, or linear algebra **c (1) :** characterized by an emphasis on line ⟨~ art⟩ **(2) :** composed of simply drawn lines with little attempt at pictorial representation ⟨~ script⟩ **d :** consisting of a straight chain of atoms **2 :** elongated with nearly parallel sides ⟨~ leaf⟩ **3 :** having or being a response or output that is directly proportional to the input **4 :** of, relating to, or based or depending on sequential development ⟨~ thinking⟩ ⟨a ~ narrative⟩ — **lin·ear·i·ty** \ˌlin-ē-ˈar-ət-ē\ *n* — **lin·ear·ly** \ˈlin-ē-ər-lē\ *adv*
Linear A \-ˈā\ *n* (1948) **:** a linear form of writing used in Crete from the 18th to the 15th centuries B.C.
linear accelerator *n* (1945) **:** a device in which charged particles are accelerated in a straight line by successive impulses from a series of electric fields
linear algebra *n* (ca. 1891) **1 :** a branch of mathematics that is concerned with mathematical structures closed under the operations of addition and scalar multiplication and with their applications and that includes the theory of systems of linear equations, matrices, determinants, vector spaces, and linear transformations **2 :** a mathematical ring which is also a vector space with scalars from an associated field and whose multiplicative operation is such that $(aA)(bB) = (ab)(AB)$ where a and b are scalars and A and B are vectors — called also *algebra*
Linear B \-ˈbē\ *n* (1948) **:** a linear form of writing employing syllabic characters and used at Knossos on Crete and on the Greek mainland from the 15th to the 12th centuries B.C. for documents in the Mycenaean language
linear combination *n* (1960) **:** a mathematical entity (as $4x + 5y + 6z$) which is composed of sums and differences of elements (as variables, matrices, or functions) whose coefficients are not all zero
linear dependence *n* (1955) **:** the property of one set (as of matrices or vectors) of having at least one linear combination of its elements equal to zero when the coefficients are taken from another given set and at least one of its coefficients is not equal to zero — **linearly dependent** *adj*
linear differential equation *n* (ca. 1890) **:** a differential equation of the first degree with respect to the dependent variable or variables and their derivatives
linear equation *n* (1816) **:** an equation of the first degree in any number of variables
linear function *n* (ca. 1889) **1 :** a mathematical function in which the variables appear only in the first degree, are multiplied by constants, and are combined only by addition and subtraction **2 :** LINEAR TRANSFORMATION
linear independence *n* (1967) **:** the property of a set (as of matrices or vectors) of having no linear combination of all its elements equal to zero when coefficients are taken from a given set unless the coefficient of each element is zero — **linearly independent** *adj*
lin·ear·ize \ˈlin-ē-ə-ˌrīz\ *vt* **-ized; -iz·ing** (1895) **:** to give a linear form to; *also* **:** to project in linear form — **lin·ear·iza·tion** \ˌlin-ē-ə-rə-ˈzā-shən\ *n*
linear measure *n* (ca. 1890) **1 :** a measure of length **2 :** a system of measures of length
linear motor *n* (1957) **:** a motor that produces thrust in a straight line by direct induction rather than with the use of gears
linear perspective *n* (1656) **:** representation in a drawing or painting of parallel lines as converging in order to give the illusion of depth and distance

EXHIBIT E-5

'S

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thromb- *or* **thrombo-** *comb form* [Gk *thrombos* clot — more at ATROPHY] : blood clot : clotting of blood ⟨*thrombin*⟩ ⟨*thromboplastic*⟩
throm·bin \'thräm-bən\ *n* [ISV] (1898) : a proteolytic enzyme that is formed from prothrombin and facilitates the clotting of blood by catalyzing conversion of fibrinogen to fibrin
throm·bo·cyte \-bə-ˌsīt\ *n* [ISV] (ca. 1910) : BLOOD PLATELET; *also* : an invertebrate cell with similar function — **throm·bo·cyt·ic** \ˌthräm-bə-'sit-ik\ *adj*
throm·bo·cy·to·pe·nia \ˌthräm-bə-ˌsīt-ə-'pē-nē-ə, -nyə\ *n* [NL, fr. ISV *thrombocyte* + Gk *penia* poverty, lack; perh. akin to L *sponte* voluntarily — more at SPIN] (ca. 1925) : persistent decrease in the number of blood platelets that is usu. associated with hemorrhagic conditions — **throm·bo·cy·to·pe·nic** \-nik\ *adj*
throm·bo·em·bo·lism \ˌthräm-bō-'em-bə-ˌliz-əm\ *n* (ca. 1935) : the blocking of a blood vessel by a particle that has broken away from a blood clot at its site of formation — **throm·bo·em·bol·ic** \-em-'bäl-ik\ *adj*
throm·bo·ki·nase \ˌthräm-bō-'kī-ˌnās, -ˌnāz\ *n* [ISV] (1908) : THROMBOPLASTIN
throm·bo·phle·bi·tis \-fli-'bīt-əs\ *n* [NL] (ca. 1890) : inflammation of a vein with formation of a thrombus
throm·bo·plas·tic \ˌthräm-bō-'plas-tik\ *adj* [ISV] (1912) : initiating or accelerating the clotting of blood
throm·bo·plas·tin \-'plas-tən\ *n* [ISV, fr. *thromboplastic*] (1914) : a complex enzyme found esp. in blood platelets that functions in the clotting of blood
throm·bo·sis \thräm-'bō-səs, thrəm-\ *n, pl* **-bo·ses** \-ˌsēz\ [NL, fr. Gk *thrombōsis* clotting, deriv. of *thrombos* clot — more at ATROPHY] (ca. 1860) : the formation or presence of a blood clot within a blood vessel during life — **throm·bot·ic** \-'bät-ik\ *adj*
throm·box·ane \thräm-'bäk-ˌsān\ *n* [*thromb-* + *ox-* + *-ane*] (1976) : any of several potent regulators of cellular function that were first isolated from thrombocytes
throm·bus \'thräm-bəs\ *n, pl* **throm·bi** \-ˌbī, -ˌbē\ [NL, fr. Gk *thrombos* clot] (ca. 1693) : a clot of blood formed within a blood vessel and remaining attached to its place of origin — compare EMBOLUS
[1]**throne** \'thrōn\ *n* [ME *trone, throne,* fr. OF *trone,* fr. L *thronus,* fr. Gk *thronos* — more at FIRM] (13c) **1 a** : the chair of state of a king, prince, or bishop **b** : the seat of a deity **2** : royal power and dignity : SOVEREIGNTY **3** *pl* : an order of angels — see CELESTIAL HIERARCHY
[2]**throne** *vb* **throned; thron·ing** *vt* (14c) **1** : to seat on a throne **2** : to invest with kingly rank or power ~ *vi* **1** : to sit on a throne **2** : to hold kingly power
throne room *n* (1864) : a formal audience room containing the throne of a sovereign
[1]**throng** \'thrȯŋ\ *n* [ME *thrang, throng,* fr. OE *thrang, gethrang;* akin to OE *thringan* to press, crowd, OHG *dringan,* Lith *trenkti* to jolt, L *truncus* trunk, torso] (bef. 12c) **1 a** : a multitude of assembled persons **b** : a large number : HOST **2 a** : a crowding together of many persons **b** : PRESSURE ⟨this ~ of business —S. R. Crockett⟩ *syn* see CROWD
[2]**throng** *vb* **thronged; throng·ing** \'thrȯŋ-iŋ\ *vt* (1534) **1** : to crowd upon : PRESS **2** : to crowd into : PACK ⟨shoppers ~*ing* the streets⟩ ~ *vi* : to crowd together in great numbers
thros·tle \'thräs-əl\ *n* [ME, fr. OE — more at THRUSH] (bef. 12c) : [1]THRUSH 1; *specif* : SONG THRUSH
[1]**throt·tle** \'thrät-ᵊl\ *vb* **throt·tled; throt·tling** \'thrät-liŋ, -ᵊl-iŋ\ [ME *throtlen,* fr. *throte* throat] *vt* (15c) **1 a** (1) : to compress the throat of : CHOKE (2) : to kill by such action **b** : to prevent or check expression or activity of : SUPPRESS **2 a** : to decrease the flow of (as steam or fuel to an engine) by a valve **b** : to regulate and esp. to reduce the speed of (as an engine) by such means **c** : to vary the thrust of (a rocket engine) during flight ~ *vi* : to throttle something (as an engine) — usu. used with *back* or *down* ⟨the pilot *throttled* back⟩ — **throt·tler** \-lər, -ᵊl-ər\ *n*
[2]**throttle** *n* [perh. alter. of E dial. *thropple* (throat)] (1547) **1 a** : THROAT 1a **b** : TRACHEA 1 **2 a** : a valve for regulating the supply of a fluid (as steam) to an engine; *esp* : the valve controlling the volume of vaporized fuel charge delivered to the cylinders of an internal-combustion engine **b** : the lever controlling this valve **c** : the condition of being throttled — **at full throttle** : at full speed
throt·tle·able \'thrät-ᵊl-ə-bəl\ *adj* (1963) : capable of having the thrust varied — used of a rocket engine
throt·tle·hold \'thrät-ᵊl-ˌhōld\ *n* (1935) : a vicious, strangling, or stultifying control
[1]**through** \(')thrü\ *prep* [ME *thurh, thruh, through,* fr. OE *thurh;* akin to OHG *durh* through, L *trans* across, beyond, Skt *tarati* he crosses over] (bef. 12c) **1 a** (1) — used as a function word to indicate movement into at one side or point and out at another and esp. the opposite side of ⟨drove a nail ~ the board⟩ (2) : by way of ⟨left ~ the door⟩ (3) — used as a function word to indicate passage from one end or boundary to another ⟨a highway ~ the forest⟩ ⟨a road ~ the desert⟩ (4) : without stopping for : PAST ⟨drove ~ a red light⟩ **b** — used as a function word to indicate passage into and out of a treatment, handling, or process ⟨the matter has already passed ~ his hands⟩ **2** — used as a function word to indicate means, agency, or intermediacy: as **a** : by means of : by the agency of **b** : because of ⟨failed ~ ignorance⟩ **c** : by common descent from or relationship with ⟨related ~ their grandfather⟩ **3 a** : over the whole surface or extent of : THROUGHOUT ⟨homes scattered ~ the valley⟩ **b** — used as a function word to indicate movement within a large expanse ⟨flew ~ the air⟩ **c** — used as a function word to indicate exposure to a specified set of conditions ⟨put her ~ hell⟩ **4** — used as a function word to indicate a period of time: as **a** : during the entire period of ⟨all ~ her life⟩ **b** : from the beginning to the end of ⟨the tower stood ~ the earthquake⟩ **c** : to and including ⟨Monday ~ Friday⟩ **5 a** — used as a function word to indicate completion or exhaustion ⟨got ~ the book⟩ ⟨went ~ a fortune in a year⟩ **b** — used as a function word to indicate acceptance or approval esp. by an official body ⟨got the bill ~ the legislature⟩
[2]**through** \'thrü\ *adv* (bef. 12c) **1** : from one end or side to the other **2 a** : from beginning to end **b** : to completion, conclusion, or accomplishment ⟨see it ~⟩ **3** : to the core : COMPLETELY ⟨soaked ~⟩ **4** : into the open : OUT ⟨break ~⟩
[3]**through** \'thrü\ *adj* (1523) **1 a** : extending from one surface to another ⟨a ~ mortise⟩ **b** : admitting free or continuous passage : DIRECT ⟨a ~ road⟩ **2 a** (1) : going from point of origin to destination without change or reshipment ⟨a ~ train⟩ (2) : of or relating to such movement ⟨a ~ ticket⟩ **b** : initiated at and destined for points outside a local zone ⟨~ traffic⟩ **3 a** : arrived at completion or accomplishment ⟨he is ~ with the job⟩ **b** : WASHED-UP, FINISHED
through and through *adv* (15c) : in every way : THOROUGHLY
through–com·posed \ˌthrü-kəm-'pōzd\ *adj* [trans. of G *durchkomponiert*] *of a song* (ca. 1903) : having new music provided for each stanza — compare STROPHIC
through·ith·er *or* **through·oth·er** \'thrü-(ə-)t͟hər\ *adv* [[1]*through* + *other*] *chiefly Scot* (1596) : in confusion : PROMISCUOUSLY
through·ly \'thrü-lē\ *adv, archaic* (15c) : in a thorough manner
[1]**through·out** \thrü-'au̇t\ *adv* (bef. 12c) **1** : in or to every part : EVERYWHERE ⟨of one color ~⟩ **2** : during the whole time or action : from beginning to end ⟨remained loyal ~⟩
[2]**throughout** *prep* (bef. 12c) **1** : all the way from one end to the other of : in or to every part of ⟨cities ~ the United States⟩ **2** : during the whole course or period of ⟨troubled him ~ his life⟩
through·put \'thrü-ˌpu̇t\ *n* (1922) : OUTPUT, PRODUCTION ⟨the ~ of a computer⟩
through street *n* (1930) : a street on which the through movement of traffic is given preference
through·way *var of* THRUWAY
throve *past of* THRIVE
[1]**throw** \'thrō\ *vb* **threw** \'thrü\; **thrown** \'thrōn\; **throw·ing** [ME *thrawen, throwen* to cause to twist, throw, fr. OE *thrāwan* to cause to twist or turn; akin to OHG *drāen* to turn, L *terere* to rub, Gk *tribein* to rub, *tetrainein* to bore, pierce] *vt* (14c) **1 a** : to propel through the air by a forward motion of the hand and arm ⟨~ a baseball⟩ **b** : to propel through the air in any manner ⟨a rifle that can ~ a bullet five miles⟩ **2 a** : to cause to fall ⟨*threw* his opponent⟩ **b** : to cause to fall off : UNSEAT ⟨the horse *threw* his rider⟩ **c** : to get the better of : OVERCOME ⟨the problem didn't ~ her⟩ **3 a** : to fling (oneself) precipitately ⟨*threw* himself down on the sofa⟩ **b** : to drive or impel violently : DASH ⟨the ship was *thrown* on a reef⟩ **4 a** (1) : to put in a particular position or condition ⟨*threw* her arms around him⟩ (2) : to put on or off hastily or carelessly ⟨*threw* on a coat⟩ **b** : to bring to bear : EXERT ⟨*threw* all his influence into the boy's defense⟩ **c** : BUILD, CONSTRUCT ⟨*threw* a pontoon bridge over the river⟩ **5** : to form or shape on a potter's wheel **6** : to deliver (a blow) in or as if in boxing **7** : to twist two or more filaments of into a thread or yarn **8 a** : to make a cast of (dice or a specified number on dice) **b** : ROLL 1a ⟨~ a bowling ball⟩ **9** : to give up : ABANDON **10** : to send forth : PROJECT ⟨the setting sun *threw* long shadows⟩ **11** : to make (oneself) dependent : commit (oneself) for help, support, or protection ⟨*threw* himself on the mercy of the court⟩ **12** : to indulge in : give way to ⟨*threw* a temper tantrum⟩ **13** : to bring forth : give birth to : SIRE, PRODUCE ⟨~s a good crop⟩ ⟨*threw* large litters⟩ **14** : to lose intentionally ⟨~ a game⟩ **15** : to move (a lever) so as to connect or disconnect parts of a clutch or switch; *also* : to make or break (a connection) with a lever **16** : to give by way of entertainment ⟨~ a party⟩ ~ *vi* : CAST, HURL — **throw·er** \'thrō(-ə)r\ *n*

syn THROW, CAST, TOSS, FLING, HURL, PITCH, SLING mean to cause to move swiftly through space by a propulsive movement or a propelling force. THROW is general and interchangeable with the other terms but may specif. imply a distinctive motion with bent arm; CAST usu. implies lightness in the thing thrown and sometimes a scattering; TOSS suggests a light or careless or aimless throwing and may imply an upward motion; FLING stresses a violent throwing; HURL implies power as in throwing a massive weight; PITCH suggests throwing carefully at a target; SLING stresses either the use of whirling momentum in throwing or directness of aim.

— **throw one's weight around** *or* **throw one's weight about** : to exercise influence or authority esp. to an excessive degree or in an objectionable manner — **throw together** **1** : to put together in a hurried and usu. careless manner ⟨a bookshelf hastily *thrown together*⟩ **2** : to bring into casual association ⟨different kinds of people are *thrown together* —Richard Sennett⟩
[2]**throw** *n* (ca. 1530) **1 a** : an act of throwing, hurling, or flinging **b** (1) : an act of throwing dice (2) : the number thrown with a cast of dice **c** : a method of throwing an opponent in wrestling or judo **2** : the distance a missile may be thrown or light rays may be projected **3** : an undertaking involving chance or danger : RISK, VENTURE **4** : the amount of vertical displacement produced by a geological fault **5 a** : the extreme movement given to a pivoted or reciprocating piece by a cam, crank, or eccentric : STROKE **b** : the length of the radius of a crank or the virtual crank radius of an eccentric or cam **6 a** : a light coverlet (as for a bed) **b** : a woman's scarf or light wrap **7** : an object or individual regarded as a distinct member of a kind or class : UNIT ⟨copies are to be sold at $5 a ~ —Harvey Breit⟩
[1]**throw·away** \'thrō-ə-ˌwā\ *n* (1903) **1** : one that is or is designed to be thrown away: as **a** : a free handbill or circular **b** : a line of dialogue (as in a play) de-emphasized by casual delivery **2** : something made or done without care or interest
[2]**throw·away** \ˌthrō-ə-ˌwā\ *adj* (1905) **1** : designed to be thrown away : DISPOSABLE ⟨~ containers⟩ **2** : written or spoken (as in a play) in a low-key or unemphatic manner ⟨~ lines⟩ **3** : NONCHALANT, CASUAL
throw away \ˌthrō-ə-'wā\ *vt* (1530) **1 a** : to get rid of as worthless or unnecessary **b** : DISCARD 1b **2 a** : to use in a foolish or wasteful manner : SQUANDER **b** : to fail to take advantage of : WASTE **3** : to make (as a line in a play) unemphatic by casual delivery
throw·back \'thrō-ˌbak\ *n* (1889) **1 a** : reversion to an earlier type or phase : ATAVISM **b** : an instance or product of atavistic reversion **c** : one that is suggestive of or suited to an earlier time or style ⟨his manners were a ~ to a more polite era⟩ **2** : FLASHBACK
throw back \(')thrō-'bak\ *vt* (1840) **1** : to delay the progress or advance of : CHECK **2** : to cause to rely : make dependent ⟨they are *thrown back* upon . . . native intelligence —Michael Novak⟩ **3** : REFLECT ~ *vi* : to revert to an earlier type or phase
throw down *vt* (14c) **1** : to cause to fail : OVERTHROW **2** : PRECIPITATE **3** : to cast off : DISCARD
throw–in \'thrō-ˌin\ *n* (1898) : an act or instance of throwing a ball in: as **a** : a throw made from the touchline in soccer to put the ball back in play after it has gone into touch **b** : a throw made by an outfielder

EXHIBIT E-6

'S

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se·quen·cy \'sē-kwən-sē\ *n* [LL *sequentia*] (1818) : SEQUENCE 3a, 5

se·quent \'sē-kwənt\ *adj* [L *sequent-, sequens,* prp.] (1601) **1** : CONSECUTIVE, SUCCEEDING **2** : CONSEQUENT, RESULTANT

se·quen·tial \si-'kwen-chəl\ *adj* (1854) **1** : of, relating to, or arranged in a sequence : SERIAL ⟨~ file systems⟩ **2** : following in sequence **3** : relating to or based on a method of testing a statistical hypothesis that involves examination of a sequence of samples for each of which the decision is made to accept or reject the hypothesis or to continue sampling — **se·quen·tial·ly** \-'kwench-(ə-)lē\ *adv*

¹**se·ques·ter** \si-'kwes-tər\ *vt* **-tered; -ter·ing** \-t(ə-)riŋ\ [ME *sequestren,* fr. MF *sequestrer,* fr. LL *sequestrare* to surrender for safekeeping, set apart, fr. L *sequester* agent, depositary, bailee; akin to L *sequi* to follow] (14c) **1** **a** : to set apart : SEGREGATE **b** : SECLUDE, WITHDRAW **2** **a** : to seize esp. by a writ of sequestration **b** : to place (property) in custody esp. in sequestration **3** : to hold (as a metallic ion) in solution usu. by inclusion in an appropriate coordination complex

²**sequester** *n, obs* (1604) : SEPARATION, ISOLATION

se·ques·trate \'sēk-wəs-,trāt, 'sek-; si-'kwes-\ *vt* **-trat·ed; -trat·ing** [LL *sequestratus,* pp. of *sequestrare*] (1513) : SEQUESTER

se·ques·tra·tion \,sēk-wəs-'trā-shən, ,sek-; (,)sē-,kwes-\ *n* (15c) **1** : the act of sequestering : the state of being sequestered **2** **a** : a legal writ authorizing a sheriff or commissioner to take into custody the property of a defendant who is in contempt until he complies with the orders of a court **b** : a deposit whereby a neutral depositary agrees to hold property in litigation and to restore it to the party to whom it is adjudged to belong

se·ques·trum \si-'kwes-trəm\ *n, pl* **-trums** *also* **-tra** \-trə\ [NL, fr. L, legal sequestration; akin to L *sequester* bailee] (1831) : a fragment of dead bone detached from adjoining sound bone

se·quin \'sē-kwən\ *n* [F, fr. It *zecchino,* fr. *zecca* mint, fr. Ar *sikkah* die, coin] (1582) **1** : an old gold coin of Italy and Turkey **2** : a small plate of shining metal or plastic used for ornamentation esp. on clothing

se·quined *or* **se·quinned** \-kwənd\ *adj* (1582) : ornamented with or as if with sequins

se·qui·tur \'sek-wət-ər, -wə-,tu̇(ə)r\ *n* [L, it follows, 3d pers. sing. pres. indic. of *sequi* to follow — more at SUE] (1836) : the conclusion of an inference : CONSEQUENCE

se·quoia \si-'kwȯi-(y)ə\ *n* [NL, genus name, fr. *Sequoya* (George Guess)] (ca. 1866) : either of two huge coniferous California trees of the pine family that reach a height of over 300 feet: **a** : BIG TREE **b** : REDWOOD 3a

sera *pl of* SERUM

se·rac \sə-'rak, sā-\ *n* [F *sérac,* lit., a kind of white cheese, fr. ML *seracium* whey, fr. L *serum* whey — more at SERUM] (1860) : a pinnacle, sharp ridge, or block of ice among the crevasses of a glacier

se·ra·glio \sə-'ral-(,)yō, -'räl-\ *n, pl* **-glios** [It *serraglio* enclosure, seraglio, partly fr. ML *serraculum* enclosure, bar of a door, bolt, fr. LL *serare* to bolt; partly fr. Turk *saray* palace — more at SEAR] (1588) **1** : HAREM 1a **2** : a palace of a sultan

se·rai \sə-'rī\ *n* [Turk & Per; Turk *saray* mansion, palace, fr. Per *sarāī* mansion, inn] (1609) **1** : CARAVANSARY **2** : SERAGLIO 2

ser·al \'sir-əl\ *adj* (1916) : of, relating to, or constituting an ecological sere

se·ra·pe \sə-'räp-ē, -'rap-\ *n* [MexSp *sarape*] (1834) : a colorful woolen shawl worn over the shoulders esp. by Mexican men

ser·aph \'ser-əf\ *n, pl* **ser·a·phim** \-ə-,fim\ *or* **seraphs** [back-formation fr. *seraphim*] (1667) : SERAPHIM 2

ser·a·phim \'ser-ə-,fim\ *n pl* [LL *seraphim,* pl., seraphs, fr. Heb *śĕrāphīm*] (bef. 12c) **1** : an order of angels — see CELESTIAL HIERARCHY **2** *sing, pl* **seraphim** : one of the 6-winged angels standing in the presence of God — **se·raph·ic** \sə-'raf-ik\ *adj* — **se·raph·i·cal·ly** \-i-k(ə-)lē\ *adv*

Se·ra·pis \sə-'rā-pəs\ *n* [L, fr. Gk *Sarapis*] : an Egyptian god combining attributes of Osiris and Apis and having a widespread cult throughout Greece and Rome

Serb \'sərb\ *n* [Serb *Srb*] (1860) **1** : a native or inhabitant of Serbia **2** : SERBIAN 2 — **Serb** *adj*

Ser·bi·an \'sər-bē-ən\ *n* (1848) **1** : SERB 1 **2** **a** : the Serbo-Croatian language as spoken in Serbia **b** : a literary form of Serbo-Croatian using the Cyrillic alphabet — **Serbian** *adj*

Ser·bo–Cro·atian \,sər-(,)bō-krō-'ā-shən\ *n* (1883) **1** : the Slavic language of the Serbs and Croats consisting of Serbian written in the Cyrillic alphabet and Croatian written in the Roman alphabet **2** : one whose native language is Serbo-Croatian — **Serbo–Croatian** *adj*

¹**sere** \'si(ə)r\ *adj* [ME, fr. OE *sēar* dry; akin to OHG *sōrēn* to wither, Gk *hauos* dry] (bef. 12c) **1** : being dried and withered **2** *archaic* : THREADBARE

²**sere** *n* [L *series* series] (1916) : a series of ecological communities formed in ecological succession

¹**ser·e·nade** \,ser-ə-'nād\ *n* [F *sérénade,* fr. It *serenata,* fr. *sereno* clear, calm (of weather), fr. L *serenus* serene] (1649) **1** **a** : a complimentary vocal or instrumental performance; *esp* : one given outdoors at night for a woman **b** : a work so performed **2** : an instrumental composition in several movements, written for a small ensemble, and midway between the suite and the symphony in style

²**serenade** *vb* **-nad·ed; -nad·ing** *vt* (1672) : to perform a serenade in honor of ~ *vi* : to play a serenade — **ser·e·nad·er** *n*

ser·e·na·ta \,ser-ə-'nät-ə\ *n* [It, serenade] (ca. 1724) : an 18th century secular cantata of a dramatic character usu. composed in honor of an individual or event

ser·en·dip·i·tous \,ser-ən-'dip-ət-əs\ *adj* (1943) : obtained or characterized by serendipity ⟨~ discoveries⟩ — **ser·en·dip·i·tous·ly** *adv*

ser·en·dip·i·ty \-'dip-ət-ē\ *n* [fr. its possession by the heroes of the Persian fairy tale *The Three Princes of Serendip*] (1754) : the faculty of finding valuable or agreeable things not sought for

¹**se·rene** \sə-'rēn\ *adj* [L *serenus;* akin to OHG *serawēn* to become dry, Gk *xēros* dry] (1503) **1** : AUGUST — used as part of a title ⟨His *Serene* Highness⟩ **2** : marked by or suggestive of utter calm and unruffled repose or quietude ⟨a ~ smile⟩ **3** **a** : clear and free of storms or unpleasant change ⟨~ skies⟩ **b** : shining bright and steady ⟨the moon, ~ in glory —Alexander Pope⟩ *syn* see CALM — **se·rene·ly** *adv* — **se·rene·ness** \-'rēn-nəs\ *n*

²**serene** *n* (1644) **1** : a serene condition or expanse (as of sky, sea, or light) **2** : SERENITY, TRANQUILLITY

se·ren·i·ty \sə-'ren-ət-ē\ *n* [ME, fr. MF *serenité,* fr. L *serenitat-, serenitas,* fr. *serenus* serene] (15c) : the quality or state of being serene

serf \'sərf\ *n* [F, fr. L *servus* slave, servant, serf — more at SERVE] (1611) : a member of a servile feudal class bound to the soil and subject to the will of his lord — **serf·age** \'sər-fij\ *n* — **serf·dom** \'sərf-dəm, -təm\ *n*

serge \'sərj\ *n* [ME *sarge,* fr. MF, fr. (assumed) VL *sarica,* fr. L *serica,* fem. of *sericus* silken — more at SERICEOUS] (14c) : a durable twilled fabric having a smooth clear face and a pronounced diagonal rib on the front and the back

ser·gean·cy \'sär-jən-sē\ *n* (1670) : the function, office, or rank of a sergeant

ser·geant \'sär-jənt\ *n* [ME, servant, attendant, sergeant, fr. MF *sergent, serjant,* fr. L *servient-, serviens,* prp. of *servire* to serve] (14c) **1** : SERGEANT AT ARMS **2** *obs* : an officer who enforces the judgments of a court or the commands of one in authority **3** : a noncommissioned officer ranking in the army and marine corps above a corporal and below a staff sergeant and in the air force above an airman first class or senior airman and below a staff sergeant; *broadly* : NONCOMMISSIONED OFFICER **4** : an officer in a police force ranking in the U.S. just below captain or sometimes lieutenant and in England just below inspector

sergeant at arms (14c) : an officer of an organization (as a legislative body or court of law) who preserves order and executes commands

sergeant first class *n* (1948) : a noncommissioned officer in the army ranking above a staff sergeant and below a master sergeant

sergeant fish *n* (ca. 1883) **1** : COBIA **2** : SNOOK 1

sergeant major *n, pl* **sergeants major** *or* **sergeant majors** (1802) **1** : a noncommissioned officer in the army, air force, or marine corps serving as chief administrative assistant in a headquarters **2** : a noncommissioned officer in the marine corps ranking above a first sergeant **3** : a bluish green to yellow percoid fish (*Abudefduf saxatilis*) with black vertical stripes on the sides that is widely distributed in the western tropical Atlantic ocean

sergeant major of the army (1966) : the ranking noncommissioned officer of the army serving as adviser to the chief of staff

sergeant major of the marine corps (ca. 1971) : the ranking noncommissioned officer of the marine corps serving as adviser to the commandant

ser·geanty \'sär-jənt-ē\ *n, pl* **-geant·ies** [ME *sergeantie,* fr. MF *sergentie,* fr. *sergent* sergeant] (15c) : any of numerous feudal services of a personal nature by which an estate is held of the king or other lord distinct from military tenure and from socage tenure

serg·ing \'sər-jiŋ\ *n* [*serge*] (ca. 1909) : the process of overcasting the raw edges of a piece of fabric (as a carpet) to prevent raveling

¹**se·ri·al** \'sir-ē-əl\ *adj* (1840) **1** : of, relating to, consisting of, or arranged in a series, rank, or row ⟨~ order⟩ **2** : appearing in successive parts or numbers ⟨a ~ story⟩ **3** : belonging to a series maturing periodically rather than on a single date ⟨~ bonds⟩ **4** : of, relating to, or being music based on a series of tones in an arbitrary but fixed pattern without regard for traditional tonality **5** : relating to or being a connection in a computer system in which the bits of a byte are transmitted sequentially over a single wire — **se·ri·al·ly** \-ə-lē\ *adv*

²**serial** *n* (1846) **1** **a** : a work appearing (as in a magazine or on television) in parts at intervals **b** : one part of a serial work : INSTALLMENT **2** : a publication (as a newspaper or journal) issued as one of a consecutively numbered and indefinitely continued series

se·ri·al·ism \'sir-ē-ə-,liz-əm\ *n* (1958) : serial music; *also* : the theory or practice of composing serial music

se·ri·al·ist \-ləst\ *n* (1846) **1** : a writer of serials **2** : a composer of serial music

se·ri·al·ize \-,līz\ *vt* **-ized; -iz·ing** (1857) : to arrange or publish in serial form — **se·ri·al·iza·tion** \,sir-ē-ə-lə-'zā-shən\ *n*

serial number *n* (1896) : a number indicating place in a series and used as a means of identification

¹**se·ri·ate** \'sir-ē-,āt, -ē-ət\ *adj* [(assumed) NL *seriatus,* fr. L *series*] (1846) : arranged in a series or succession — **se·ri·ate·ly** *adv*

²**se·ri·ate** \'sir-ē-,āt\ *vt* **-at·ed; -at·ing** (1872) : to arrange in a series

¹**se·ri·a·tim** \,sir-ē-'āt-əm, -'at-\ *adv* [ML, fr. L *series*] (1680) : in a series

²**seriatim** *adj* (1871) : following seriatim

se·ri·ceous \sə-'rish-əs\ *adj* [LL *sericeus* silken, fr. L *sericum* silk garment, silk, fr. neut. of *sericus* silken, fr. Gk *sērikos,* fr. *Sēres,* an eastern Asian people producing silk in ancient times] (ca. 1777) : finely pubescent ⟨~ leaf⟩

ser·i·cin \'ser-ə-sən\ *n* [ISV, fr. L *sericum* silk] (ca. 1868) : a gelatinous protein that cements the two fibroin filaments in a silk fiber

seri·cul·ture \'ser-ə-,kəl-chər\ *n* [L *sericum* silk + E *culture*] (1851) : the production of raw silk by raising silkworms — **seri·cul·tur·al** \-'kəlch(-ə)-rəl\ *adj* — **seri·cul·tur·ist** \-rəst\ *n*

se·ries \'si(ə)r-(,)ēz\ *n, pl* **series** *often attrib* [L, fr. *serere* to join, link together; akin to L *sort-, sors* lot, Gk *eirein* to string together, *hormos* chain, necklace] (1611) **1** **a** : a number of things or events of the same class coming one after another in spatial or temporal succession ⟨a concert ~⟩ ⟨the hall opened into a ~ of small rooms⟩ **b** : a set of regularly presented television programs each of which is complete in itself **2** : the indicated sum of a usu. infinite sequence of numbers **3** **a** : the coins or currency of a particular country and period **b** : a group of postage stamps in different denominations **4** : a succession of volumes or issues published with related subjects or authors, similar format and price, or continuous numbering **5** : a division of rock formations that is smaller than a system and comprises rocks deposited during an epoch **6** : a group of chemical compounds related in composition and structure **7** : an arrangement of the parts of or elements in an electric circuit whereby the whole current passes through each part or element without branching **8** : a set of vowels connected by ablaut (as *i, a, u* in *ring, rang, rung*) **9** **a** : a number of games (as of baseball) played usu. on consecutive days between two teams ⟨in town for a 3-game ~⟩ **b** : WORLD SERIES **10** : a group of successive coordinate sentence elements joined together **11** : SOIL SERIES **12** : three consecutive games in bowling — **in series** : in a serial arrangement

series winding *n* (ca. 1909) : a winding in which the armature coil and the field-magnet coil are in series with the external circuit — **se·ries–wound** \,sir-ēz-'wau̇nd\ *adj*

EXHIBIT I-2

US006573968B2

(12) **United States Patent**
Jeong

(10) **Patent No.: US 6,573,968 B2**
(45) **Date of Patent: Jun. 3, 2003**

(54) **SEAL PATTERN FOR LIQUID CRYSTAL DISPLAY DEVICE AND RELATED METHOD**

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(73) Assignee: **LG. Philips LCD Co., Ltd.**, Seoul (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 347 days.

(21) Appl. No.: **09/737,766**

(22) Filed: **Dec. 18, 2000**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Dec. 16, 1999 (KR) 1999-58106

(51) **Int. Cl.**[7] **G02F 1/1336**
(52) **U.S. Cl.** **349/153**
(58) **Field of Search** 349/153, 154, 349/187, 189, 190

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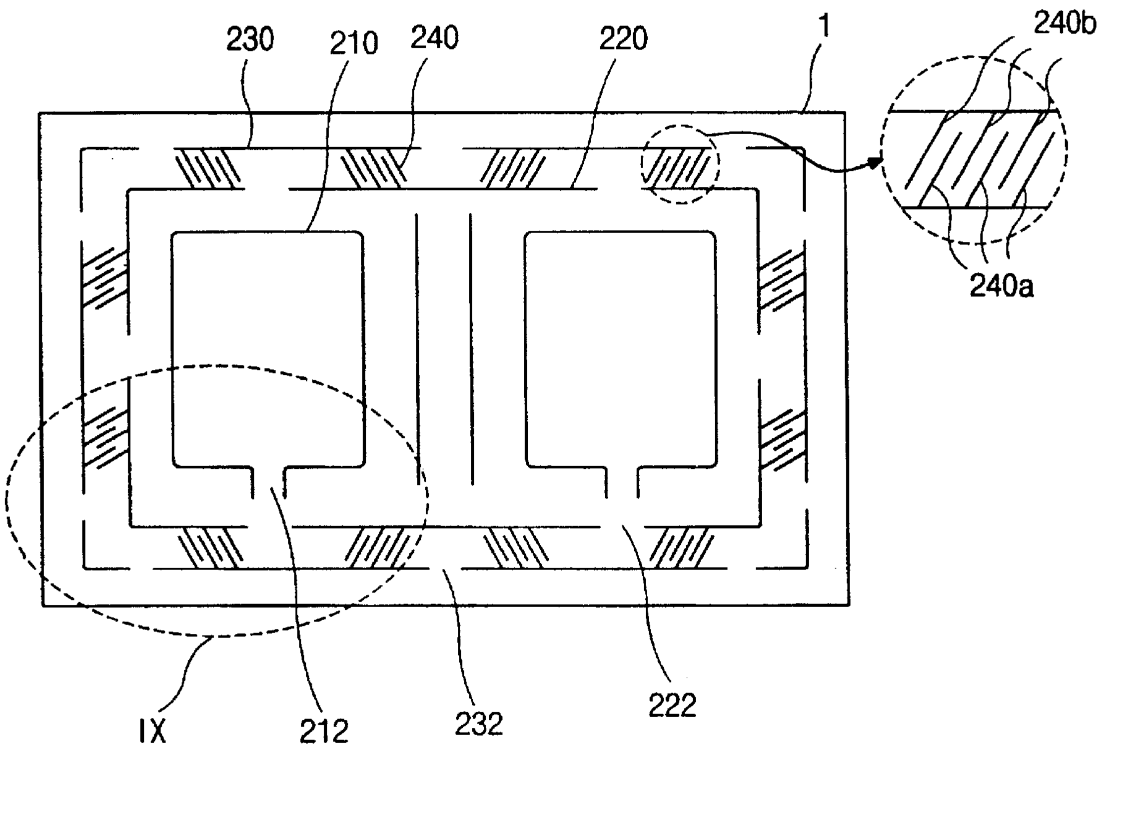
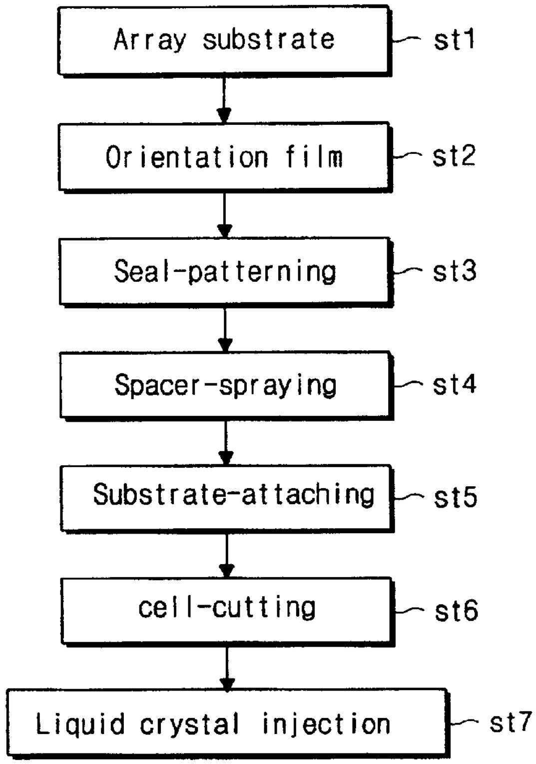
(57) **ABSTRACT**

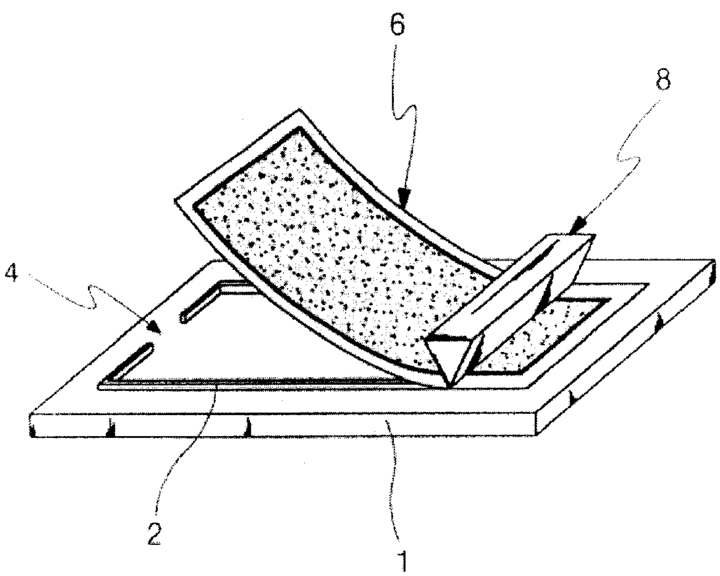
A seal pattern includes a plurality of main seal lines, a first auxiliary seal line including a plurality of first openings and surrounding the plurality of main seal lines, a second auxiliary seal including a plurality of second openings and surrounding the first auxiliary seal line, and a plurality of third auxiliary seal lines positioned between the first and second openings. The third auxiliary seal lines pass only gas such as air and the main seal lines are protected from being damaged from a cleaning detergent or an etchant such as an HF solution during a cleaning and etching process.

54 Claims, 5 Drawing Sheets

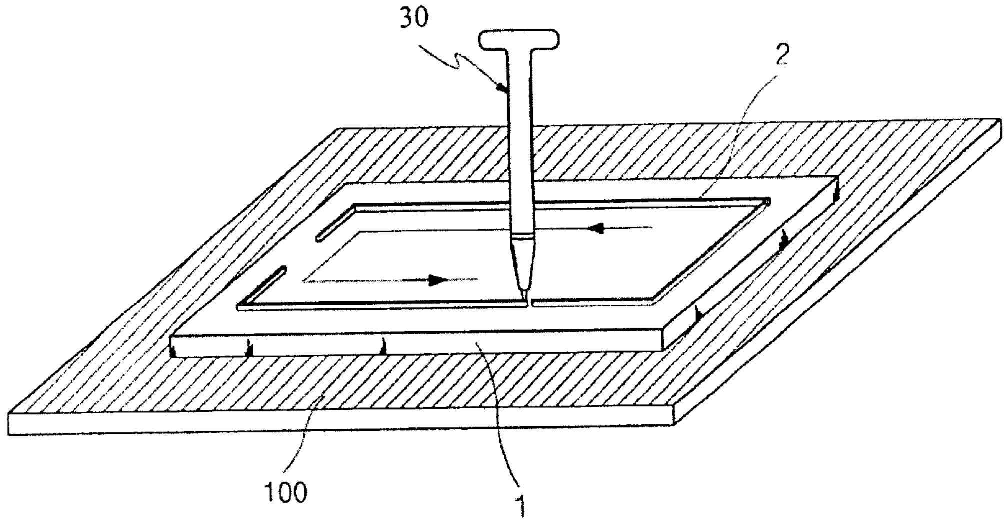




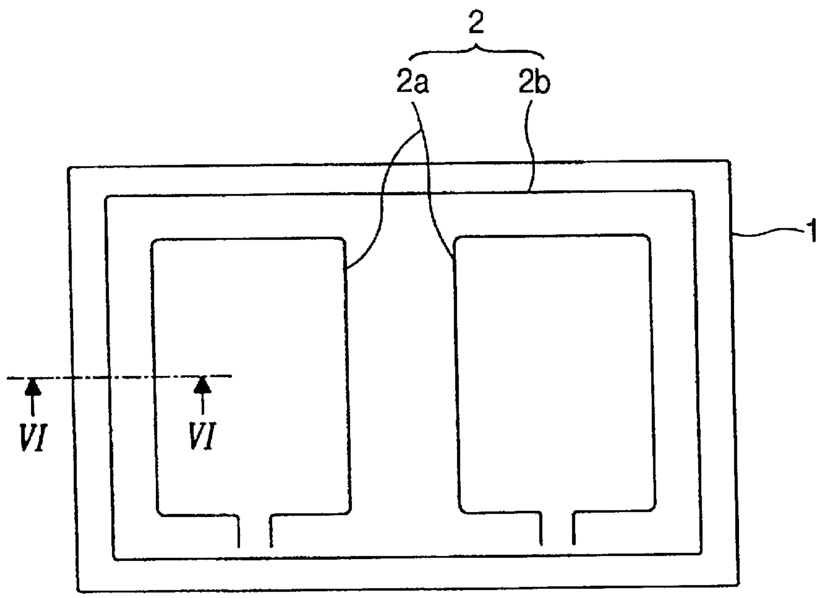
(related art)
FIG. 1



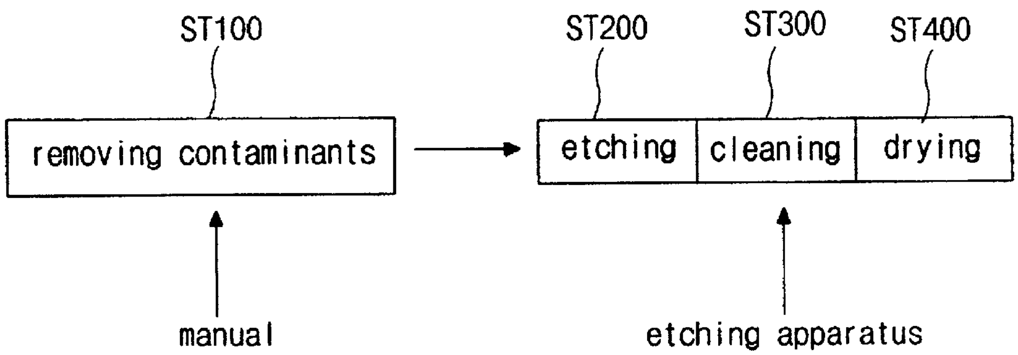
(related art)
FIG. 2



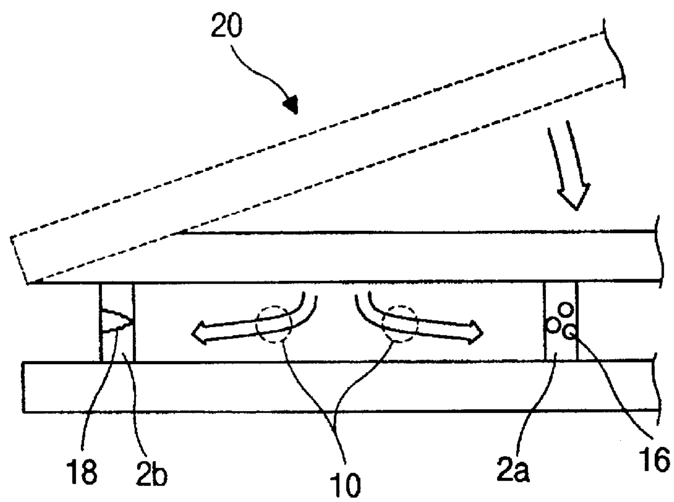
(related art)
FIG. 3



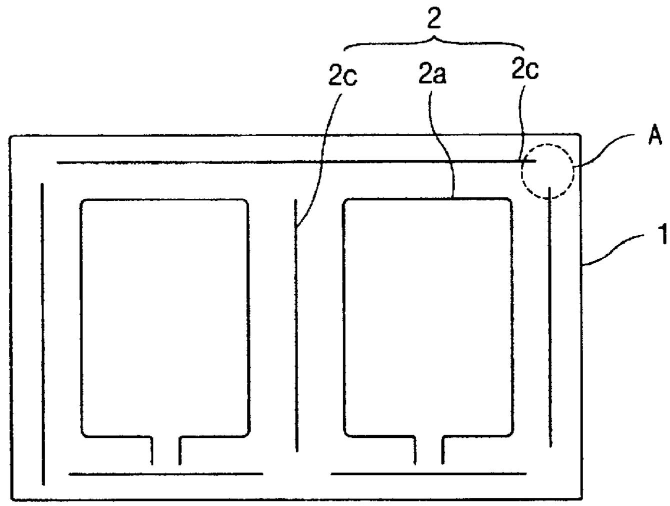
(related art)
FIG. 4



(related art)
FIG. 5



(related art)
FIG. 6



(related art)
FIG. 7

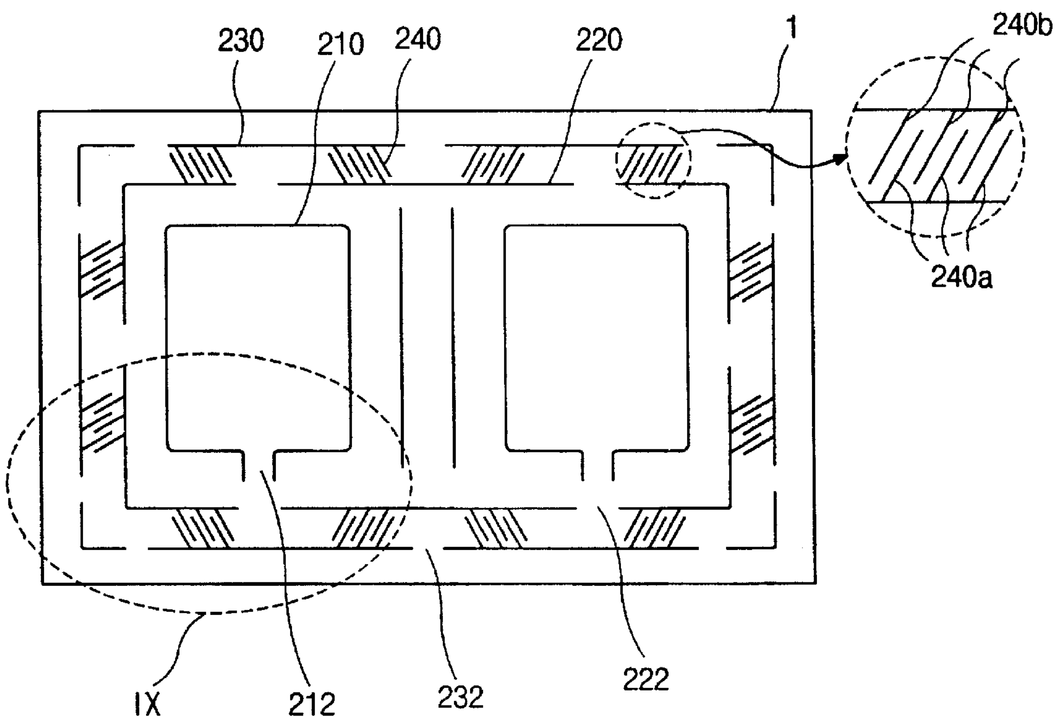


FIG. 8

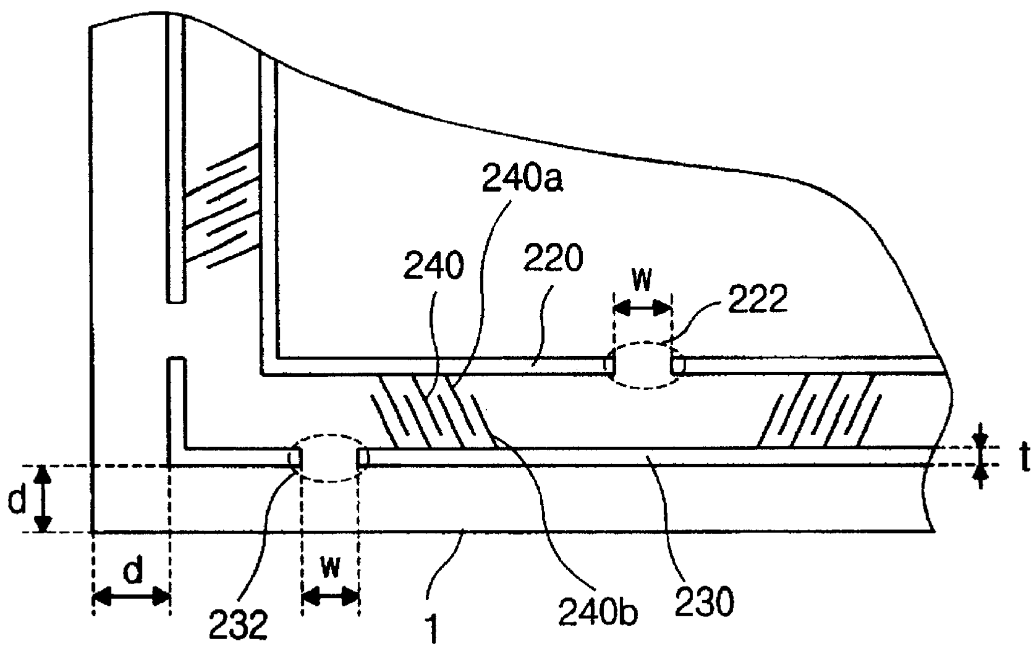


FIG. 9

SEAL PATTERN FOR LIQUID CRYSTAL DISPLAY DEVICE AND RELATED METHOD

This application claims the benefit of Korean Patent Application No. 1999-58106, filed on Dec. 16, 1999, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to a seal pattern for a liquid crystal display and a method of manufacturing the same.

2. Discussion of the Related Art

Recently, liquid crystal display (LCD) devices with light, thin, low power consumption characteristics have been used, for example, in office automation (OA) equipments and video units. A typical liquid crystal display (LCD) panel has upper and lower substrates and an interposed liquid crystal layer. The upper substrate usually includes common electrodes, while the lower substrate includes switching elements, such as thin film transistors (TFTs), and pixel electrodes.

As the present invention relates to manufacturing liquid crystal display panels, a brief explanation of conventional liquid crystal display manufacturing processes will be discussed. Common electrodes and pixel electrodes are formed on upper and lower substrates, respectively. A seal is then formed on the lower substrate. The upper and lower substrates are then bonded together using the seal such that the common electrodes of the upper substrate and the pixel electrodes of the lower substrate face each other, forming liquid crystal cells. Liquid crystal material is then injected into those cells through injection holes. The injection holes are then sealed. Finally, polarizing films are attached to the outer surfaces of the upper and lower substrates.

The pixel and common electrodes generate electric fields that control the light passing through the liquid crystal cells. By controlling the electric fields desired characters or images are displayed.

While fabricating the various components of a liquid crystal display, such as the thin film transistors or the color filters, typically requires numerous manufacturing steps, the overall fabrication process is relatively straightforward. FIG. **1** illustrates a typical liquid crystal panel manufacturing process in some detail. Step st**1** forms an array matrix of thin film transistors and pixel electrodes over an array (lower) substrate.

Step st**2** forms an orientation film over the lower substrate. This involves uniformly depositing a polymer thin film over the lower substrate and then uniformly rubbing the polymer thin film with a fabric. The rubbing process involves rubbing the surface of the polymer thin film to orientate or align the film. A typical orientation film is an organic thin film such as a polyimide thin film.

Step st**3** produces a seal pattern on the lower substrate. When the upper and lower substrates are attached, the seal pattern forms cell spaces that will receive the liquid crystal material. The seal pattern will also prevent the interposed liquid crystal material from leaking out of the completed liquid crystal cell. A thermosetting plastic and a screen-print technology are conventionally used to fabricate the seal pattern.

Step st**4** is to spray spacers over the lower substrate. The spacers have a definite size and act to maintain a precise and uniform space between the upper and lower substrates. Accordingly, the spacers are placed with a uniform density on the lower substrate using either a wet spray method, in which case the spacers are mixed in an alcohol and then sprayed, or a dry spray method in which only the spacers are sprayed. The dry spray method is divided into a static electric spray method that uses static electricity and a non-electric spray method that uses gas pressure. Since static electricity can be harmful to the liquid crystal, the non-electric spray method is widely used.

The next step, st**5**, is to aligned and attached the upper and lower substrates together, and to attach color filters to the upper substrate and the lower substrate. The aligning margin, which is less than a few micrometers, is important. If the upper and lower substrates are aligned and attached beyond the aligning margin, light leaks away such that the liquid crystal cell cannot adequately performed its function.

Step st**6** cuts the liquid crystal element fabricated through the above five steps into individual liquid crystal cells. Conventionally, a liquid crystal material was injected into the space between the upper and the lower substrates before cutting the liquid crystal element into individual liquid crystal cells. However, as displays have become larger, the liquid crystal cells are usually cut first and then the liquid crystal material is injected. The cutting process typically includes scribing using a diamond pen to form cutting lines on a substrate, and a breaking step that separates the substrate along the scribed lines.

Step st**7** actually injects liquid crystal material into the individual liquid crystal cells. Since each individual liquid crystal cell is a few square centimeters in area, but has only a few micrometer gap between plates, a vacuum injection method is effectively and widely used. Generally, the step of injecting the liquid crystal material into the cells takes the longest manufacturing time. Thus, for manufacturing efficiency, it is important to have optimum conditions for vacuum injection.

Now, referring to FIG. **2**, the screen-print method used for the seal pattern process of the third step (st**3**) is explained.

The screen-print technology is facilitated with a patterned screen **6** and a squeegee **8**. In order to interpose the liquid crystal without leakage, the seal pattern **2** is formed along edges of a substrate **1**. At one side of the edge, an injection hole **4** for injecting the liquid crystal is formed. To form the seal pattern **2**, a thermosetting resin or an ultraviolet-setting epoxy resin and the like is deposited on the substrate **1**, and thereafter a solvent included in the sealant is evaporated for leveling.

At this point, although the epoxy resin itself is not harmful to the liquid crystal, an amine in a thermohardening solvent for forming the thermosetting resin decomposes the liquid crystal. Thus, when using the epoxy resin for the seal pattern **2**, the sealant formed through the screen-print technology should be pre-baked sufficiently with a gradual variance of the baking temperature. Further, in forming the seal pattern, the uniformity in thickness and width of the sealant are very important to maintain the uniform spacing (or gap) between the two substrates.

FIG. **3** shows a different seal-patterning technology, a dispenser-print technology. As shown, the dispenser-print technology uses a dispenser **30** filled with the sealant and a table **100** where the substrate **1** is placed. The dispenser **30** moves over the table **100** and forms the sealant according to the direction of the arrow so as to form the sealant pattern **2**.

FIG. **4** shows a conventional seal pattern formed on a substrate via the above-mentioned seal-patterning technol-

ogy. Referring to FIG. **4**, on a substrate **1**, a seal pattern **2** is formed. The seal pattern **2** includes main seal lines **2***a* and an auxiliary seal line **2***b*. As previously explained, the main seal lines **2***a* prevent the leakage of the liquid crystal, while the auxiliary seal line **2***b* surrounds the main seal lines **2***a* to protect the main seal lines **2***a* from a cleaning detergent or an etching solution during a cleaning and etching process.

The cleaning and etching process decreases the thickness of the assembled substrates. A 10% decrease in the substrate thickness result in a 20% decrease in the weight of the liquid crystal display device. FIG. **5** illustrates the cleaning and etching process in a block diagram.

Before the seventh step, st**7**, of injecting the liquid crystal shown in FIG. **1**, the assembled substrates produced from the first to sixth steps, st **1** to st **6**, shown in FIG. **1**, are cleaned manually using a cleaning detergent such as isopropyl alcohol (IPA) or deionized water (DI water). Through the first cleaning step, ST **100**, contaminants such as a polymer layer or minute particles on the outer surfaces of the assembled substrates are removed.

Next, in an etching step, ST **200**, using an etching apparatus, the assembled substrates are etched in aqueous solution of hydrofluoric (HF) acid.

In a next cleaning step, ST **300**, the HF solution remaining on the assembled substrates is removed, and in a drying step, ST **400**, the assembled substrates are dried sufficiently.

Subsequently, in the seventh step, st**7**, of FIG. **1**, the liquid crystal is injected into the assembled substrates and sealed. The etching apparatus may also be used for cleaning step ST**300** and the drying step ST **400**.

As above-mentioned, during the cleaning and etching steps, ST**100** and ST**200**, the auxiliary seal line **2***b* protects the main seal lines **2***a* from the cleaning detergent or the HF solution such that the main seal lines **2***a* maintain their structure. However, the auxiliary seal line **2***b* is damaged as illustrated in FIG. **6**.

Referring to FIG. **6**, when an upper substrate **20** is attached to the lower substrate **1**, air **10** existing between the main seal lines **2***a* and auxiliary seal line **2***b* is pressurized and still remains therebetween. After the attachment, since there is no open hole in the auxiliary seal line **2***b*, the pressurized air **10** can not be discharged from the assembled substrates **1** and **20**. The pressurized air **10** in the assembled substrates makes air bubbles **16** or cracks **18** in the main and auxiliary seal lines **2***a* and **2***b*. Due to the air bubbles **16** and cracks **18**, the main seal lines **2***a* can not stably seal the liquid crystal injected in a later process.

As shown in FIG. **7**, if open holes "A" are formed in auxiliary seal lines **2***c* to solve the above-mentioned problem, the cleaning detergent or HF solution penetrates into the assembled substrates in the cleaning and etching process, results in a deformation of the main seal lines **2***a*.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a seal pattern of a liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An advantage of the present invention is a seal pattern for a liquid crystal display device that prevents damage from a cleaning detergent or an etchant such as an HF solution.

Another advantage of the present invention is a seal pattern for a liquid crystal display device that allows air to flow freely.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims thereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a liquid crystal display device includes a plurality of main seal lines on a substrate; a first auxiliary seal line having a plurality of first open holes (or openings); a second auxiliary seal line having a plurality of second open holes; and third auxiliary seal lines between the first and second open holes, each of the third auxiliary seal line having first and second portions. The first auxiliary seal line surrounds the main seal lines. The second auxiliary seal line surrounds the first auxiliary seal line. The first and second portions of each of the third auxiliary seal lines are connected with the first and second auxiliary seal lines, respectively. Each of the third auxiliary seal lines has a zigzag shape. Each width of the first and second open holes is at least four times as large as each thickness of the first and second auxiliary seal lines.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. **1** is a block diagram illustrating a typical manufacturing process for a liquid crystal cell;

FIG. **2** is a perspective view illustrating a seal pattern process with a screen-print method;

FIG. **3** is a perspective view illustrating a dispenser-print method for the seal pattern;

FIG. **4** is a plane view of a conventional seal pattern printed on a substrate;

FIG. **5** is a block diagram illustrating a typical etching process for a liquid crystal panel;

FIG. **6** is a cross-sectional view of the liquid crystal display device panel taken along a line "VI—VI" shown in FIG. **4**;

FIG. **7** is a plane view of another conventional seal pattern printed on a substrate;

FIG. **8** is a plane view of a seal pattern according to a preferred embodiment of the present invention; and

FIG. **9** is an enlarged plane view of a portion "IX" of FIG. **8**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to an embodiment of the present invention, which is illustrated in the accompanying drawings.

Referring to FIG. **8**, on a substrate **1**, a plurality of main seal lines **210** are formed in a rectangular shape. At one side in each of the main seal lines **210**, an injection hole **212** is formed to open the main seal line **210**. Through the injection hole **212**, a liquid crystal will be injected (in the liquid

crystal injection step, st**7**, shown in FIG. **1**) into a space defined by the main seal lines **210**.

A first auxiliary seal line **220** is formed on the substrate **1** and surrounds the plurality of main seal lines **210** with space between the main and the auxiliary seal lines **210** and **220**. In the first auxiliary seal line **220**, a plurality of first open holes (or openings) **222** are formed to open the first auxiliary seal line **220**. The first open holes **222** should not overlap the injection holes **212** of the main seal lines **210** in its location.

A second auxiliary seal line **230** is formed on the substrate **1** and surrounds the first auxiliary seal line **220** with space between the first and the second auxiliary seal lines **220** and **230**. In the second auxiliary seal line **230**, a plurality of second open holes **232** are formed to open the second auxiliary seal line **230**. At this point, the second open holes **232** should not overlap the first open holes **222** of the first auxiliary seal line **220**. Namely, the second open holes **232** are preferably not located at corresponding portions of the first open holes **222** in the first auxiliary seal line **220**.

Between the first and second auxiliary seal lines **220** and **230**, a plurality of third auxiliary lines **240** are formed to define boundary areas between the first and the second open holes **222** and **232**. Each of the third auxiliary seal lines **240** includes a plurality of first and second seal fins **240***a* and **240***b* that are spaced apart from each other alternatively. The first and second seal fins **240***a* and **240***b* are preferably connected to the first and second auxiliary seal lines **220** and **230**, respectively.

FIG. **9** shows the structure of the first, second, and third auxiliary seal lines **220**, **230** and **240** in detail.

Referring to FIG. **9**, the second auxiliary seal line **230** is spaced apart from edges of the substrate **1** by a distance “d”. The distance “d” is preferably less than 10 mm such that the area of the substrate **1** is efficiently used. Each width “w” of the first and second open holes **222** and **232** is preferably about four times as large as each thickness “t” of the first and second auxiliary seal lines **220** and **230**.

During the substrate-attaching step, st**5**, shown in FIG. **1**, the open holes shrink such that the width “w” of the open holes become as small as or a little larger than the thickness “t” of the seal lines due to a deformation of the seal lines from pressure. If the open holes are not wide enough, the seal lines become closed after the above-mentioned substrate-attaching step, st**5**.

Still referring to FIG. **9**, the third auxiliary seal lines **240** separate the first open holes **222** from the second open holes **232**. In particular, in the space between the first and second auxiliary seal lines **220** and **230**, and between the first and second open holes **222** and **232**, there preferably always exists a third seal line **240** across the first and second seal lines **220** and **230**.

Since first and second seal fins **240***a* and **240***b* are connected to the first and the second auxiliary seal lines **220** and **230**, respectively, liquid cannot pass through the third auxiliary seal line **240** due to a surface tension of the liquid. Accordingly, in a later cleaning and etching step illustrated in FIG. **5**, a cleaning detergent or an etchant such as an HF solution cannot pass through the third auxiliary seal lines **240**, and cannot penetrate through the first auxiliary seal line **220**. Therefore, the main seal lines **210** maintain their structure and properties in a safe manner without being damaged from the cleaning detergent or the etching solution.

Since the substrates include silicon oxide (SiO_2) by 60%, there occurs a chemical reaction between the substrates and the HF solution as follows:

$$SiO_2+4HF \rightarrow SiF_4\uparrow+2H_2O+E$$

During the etching step, ST**200** (FIG. **5**), silicon oxide of the substrates is etched via the HF solution. Here, “E” is the heat of reaction that is produced during the etching step.

By measuring the heat “E” of the reaction (a reaction temperature), the etching rate is calculated. The etching step is facilitated from considering the reaction temperature. When the reaction temperature becomes equal to a reference temperature, the etching is stopped. At this point, the desired reduction in the thickness of the substrates is achieved. A more detailed explanation of the substrate etching process is contained in U.S. patent application Ser. No. 09/002,037 filed on Dec. 31, 1997, entitled “Method of Fabricating Substrate” and assigned to the same assignee as the present invention, the entirety of which is hereby incorporated by reference in this application.

However, since the first and second seal fins **240***a* and **240***b* are spaced apart from each other in an alternating manner, gas can pass through the third auxiliary seal lines **240** freely. Therefore, in the substrate-attaching step, st **5**, shown in FIG. **1**, air remaining in the space between the main seal line **210** and the first auxiliary seal lines **220** flows out through the first and second open holes **222** and **232**. Since the remaining air between the main seal lines **210** and the first auxiliary seal line **220** is not pressurized, the main seal lines **210** maintain their structure without air bubbles **16** or cracks **18** and safe from being damaged.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device comprising:

a main seal line having a main opening on a substrate;

a first auxiliary seal line having a first opening;

a second auxiliary seal line having a second opening; and

a third auxiliary seal line having first and second portions between the first and second openings.

2. The liquid crystal display device of claim **1**, wherein the first auxiliary seal line substantially surrounds the main seal lines.

3. The liquid crystal display device of claim **1**, wherein the second auxiliary seal line substantially surrounds the first auxiliary seal line.

4. The liquid crystal display device of claim **1**, wherein the third auxiliary seal line has a structure that effectively prevents liquid from penetrating through thee third auxiliary seal line due to surface tension of the liquid.

5. The liquid crystal display device of claim **1**, wherein the first and second portions of the third auxiliary seal line are connected to the first and second auxiliary seal lines, respectively.

6. The liquid crystal display device of claim **5**, wherein the first portion extends from the first auxiliary seal line in a direction toward the second auxiliary seal line, the first portion not touching the second auxiliary seal line.

7. The liquid crystal display device of claim **6**, wherein the first portion extends toward the second auxiliary line in a slanting manner.

8. The liquid crystal display device of claim **5**, wherein the second portion extends from the second auxiliary seal line in a direction toward the first auxiliary seal line, the second portion not touching the first auxiliary seal line.

9. The liquid crystal display device of claim **8**, wherein the second portion extends toward the first auxiliary line in a slanting manner.

10. The liquid crystal display device of claim **5**, wherein the first portion and second portions extend toward the second and first auxiliary lines in a slanting manner, respectively.

11. The liquid crystal display device of claim **1**, wherein the second auxiliary seal line is spaced from an edge of the substrate to allow for an efficient use of the substrate.

12. The liquid crystal display device of claim **1**, wherein the second auxiliary seal line is spaced from an edge of the substrate by less than 10 mm.

13. The liquid crystal display device of claim **1**, wherein the first opening of the first auxiliary seal line and the second opening of the second auxiliary seal line do not overlap each other at all.

14. The liquid crystal display device of claim **1**, wherein the first and second portions of the third auxiliary seal line have a zigzag shape.

15. The liquid crystal display device of claim **1**, wherein a width of the first opening in the first auxiliary seal line is large enough to be prevented from closing after attaching the substrate to a second substrate.

16. The liquid crystal display device of claim **15**, wherein the first opening is about four times as large as a thickness of the first auxiliary seal line.

17. The liquid crystal display device of claim **1**, wherein a width of the second opening in the second auxiliary seal line is large enough to be prevented from closing after attaching the substrate to a second substrate.

18. The liquid crystal display device of claim **17**, wherein the second opening is about four times as large as a thickness of the second auxiliary seal line.

19. The liquid crystal display device of claim **1**, wherein widths of the first and second openings in the first and second auxiliary seal lines are large enough to be prevented from closing after attaching the substrate to a second substrate.

20. The liquid crystal display device of claim **19**, wherein the first and second openings are at least four times as large as a thickness of the first and second auxiliary seal lines, respectively.

21. The liquid crystal display device of claim **1**, wherein the first auxiliary seal line includes a plurality of first openings.

22. The liquid crystal display device of claim **1**, wherein the second auxiliary seal line includes a plurality of second openings.

23. The liquid crystal display device of claim **1**, wherein the first opening of the first auxiliary seal line at least partially overlaps the main opening of the main seal line.

24. The liquid crystal display device of claim **1**, wherein the first auxiliary seal line includes a plurality of first openings and the second auxiliary seal line includes a plurality of second openings corresponding to the first openings, any pair of the first and second openings having the third auxiliary seal line.

25. The liquid crystal display device of claim **24**, wherein at least one of the first openings of the first auxiliary seal line at least partially overlaps the main opening of the main seal line.

26. The liquid crystal display device of claim **1**, further comprising a plurality of main seal lines, each main seal line including a main opening.

27. A method of fabricating a liquid crystal display device having first and second substrates comprising:

forming a main seal line on the first substrate;

forming a first auxiliary seal line on the first substrate, the first auxiliary seal line having a first opening;

forming a second auxiliary seal line on the first substrate, the second auxiliary seal line having a second opening;

forming a third auxiliary seal line having first and second portions on the first substrate;

attaching the first and second substrates; and

interposing a liquid crystal layer between the first and second substrates.

28. The method of claim **27**, further comprising etching a surface of at least one of the first and second substrates prior to interposing the liquid crystal between the first and second substrates.

29. The method of claim **27**, further comprising etching a surface of at least one of the first and second substrates after interposing the liquid crystal between the first and second substrates.

30. The method of claim **27**, wherein the first auxiliary seal line substantially surrounds the main seal lines.

31. The method of claim **27**, wherein the second auxiliary seal line substantially surrounds the first auxiliary seal line.

32. The method of claim **27**, wherein the third auxiliary seal line has a structure that effectively prevents liquid from penetrating through thee third auxiliary seal line due to surface tension of the liquid.

33. The method of claim **27**, wherein the first and second portions of the third auxiliary seal line are connected to the first and second auxiliary seal lines, respectively.

34. The method of claim **33**, wherein the first portion extends from the first auxiliary seal line in a direction toward the second auxiliary seal line, the first portion not touching the second auxiliary seal line.

35. The method of claim **34**, wherein the first portion extends toward the second auxiliary line in a slanting manner.

36. The method of claim **33**, wherein the second portion extends from the second auxiliary seal line in a direction toward the first auxiliary seal line, the second portion not touching the first auxiliary seal line.

37. The method of claim **36**, wherein the second portion extends toward the first auxiliary line in a slanting manner.

38. The method of claim **33**, wherein the first portion and second portions extend toward the second and first auxiliary lines in a slanting manner, respectively.

39. The method of claim **27**, wherein the second auxiliary seal line is spaced from an edge of the substrate to allow for an efficient use of the substrate.

40. The method of claim **27**, wherein the second auxiliary seal line is spaced from an edge of the substrate by less than 10 mm.

41. The method of claim **27**, wherein the first opening of the first auxiliary seal line and the second opening of the second auxiliary seal line do not overlap each other at all.

42. The method of claim **27**, wherein the first and second portions of the third auxiliary seal line have a zigzag shape.

43. The method of claim **27**, wherein a width of the first opening in the first auxiliary seal line is large enough to be prevented from closing after attaching the substrate to a second substrate.

44. The method of claim **43**, wherein the first opening is about four times as large as a thickness of the first auxiliary seal line.

45. The method of claim **27**, wherein a width of the second opening in the second auxiliary seal line is large enough to be prevented from closing after attaching the substrate to a second substrate.

46. The method of claim **45**, wherein the second opening is about four times as large as a thickness of the second auxiliary seal line.

47. The method of claim **25**, wherein widths of the first and second openings in the first and second auxiliary seal lines are large enough to be prevented from closing after attaching the substrate to a second substrate.

48. The method of claim **47**, wherein the first and second openings are at least four times as large as a thickness of the first and second auxiliary seal lines, respectively.

49. The method of claim **27**, wherein the first auxiliary seal line includes a plurality of first openings.

50. The method of claim **27**, wherein the second auxiliary seal line includes a plurality of second openings.

51. The method of claim **27**, wherein the first opening of the first auxiliary seal line at least partially overlaps the main opening of the main seal line.

52. The method of claim **27**, wherein the first auxiliary seal line includes a plurality of first openings and the second auxiliary seal line includes a plurality of second openings corresponding to the first openings, any pair of the first and second openings having the third auxiliary seal line.

53. The method of claim **52**, wherein at least one of the first openings of the first auxiliary seal line at least partially overlaps the main opening of the main seal line.

54. The method of claim **27**, further comprising a plurality of main seal lines, each main seal line including a main opening.

* * * * *

EXHIBIT I-3

Merriam-Webster's Collegiate® Dictionary

TENTH EDITION

Merriam-Webster, Incorporated
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Abbreviat

¹con·test \ˈkän-ˌtest\ *n* (1647) **1** : a struggle for superiority or victory : COMPETITION **2** : a competition in which each contestant performs without direct contact with or interference from his competitors

con·tes·tant \kən-ˈtes-tənt *also* ˈkän-ˌ\ *n* (1665) **1** : one that participates in a contest **2** : one that contests an award or decision

con·tes·ta·tion \ˌkän-ˌtes-ˈtā-shən\ *n* (1580) : CONTROVERSY, DEBATE

con·text \ˈkän-ˌtekst\ *n* [ME, weaving together of words, fr. L *contextus* connection of words, coherence, fr. *contexere* to weave together, fr. *com-* + *texere* to weave — more at TECHNICAL] (ca. 1568) **1** : the parts of a discourse that surround a word or passage and can throw light on its meaning **2** : the interrelated conditions in which something exists or occurs : ENVIRONMENT, SETTING — **con·text·less** \-ˌtekst-ləs\ *adj* — **con·tex·tu·al** \kän-ˈteks-chə-wəl, kən-, -chəl\ *adj* — **con·tex·tu·al·ly** *adv*

con·text–free \ˈkän-ˌtekst-ˈfrē\ *adj* (1964) : of, relating to, or being a grammar or language based on rules that describe a change in a string without reference to elements outside of the string; *also* : being such a rule

con·tex·tu·al·ize \kən-ˈteks-chə-wə-ˌlīz, -chə-ˌlīz\ *vt* **-ized; -iz·ing** (1934) : to place (as a word or activity) in a context

con·tex·ture \kən-ˈteks-chər, ˈkän-ˌ, kän-ˈ\ *n* [F, fr. L *contextus*, pp. of *contexere*] (1603) **1** : the act, process, or manner of weaving parts into a whole; *also* : a structure so formed ⟨a ~ of lies⟩ **2** : CONTEXT

con·ti·gu·i·ty \ˌkän-tə-ˈgyü-ə-tē\ *n, pl* **-ties** (1612) : the quality or state of being contiguous : PROXIMITY

con·tig·u·ous \kən-ˈti-gyə-wəs\ *adj* [L *contiguus*, fr. *contingere* to have contact with — more at CONTINGENT] (ca. 1609) **1** : being in actual contact : touching along a boundary or at a point **2** *of angles* : ADJACENT 2 **3** : next or near in time or sequence **4** : touching or connected throughout in an unbroken sequence ⟨~ row houses⟩ *syn* see ADJACENT — **con·tig·u·ous·ly** *adv* — **con·tig·u·ous·ness** *n*

con·ti·nence \ˈkän-tᵊn-ən(t)s\ *n* (14c) **1** : SELF-RESTRAINT; *esp* : a refraining from sexual intercourse **2** : the ability to retain a bodily discharge voluntarily ⟨fecal ~⟩

¹con·ti·nent \ˈkän-tᵊn-ənt\ *adj* [ME, fr. MF, fr. L *continent-, continens*, fr. prp. of *continēre* to hold in — more at CONTAIN] (14c) **1** : exercising continence **2** *obs* : RESTRICTIVE — **con·ti·nent·ly** *adv*

²con·ti·nent \ˈkän-tᵊn-ənt, ˈkänt-nənt\ *n* [in senses 1 & 2, fr. L *continent-, continens*, prp. of *continēre*, to hold together, contain; in senses 3 & 4, fr. L *continent-, continens* continuous mass of land, mainland, fr. *continent-, continens*, prp.] (1541) **1** *archaic* : CONTAINER, CONFINES **2** *archaic* : EPITOME **3** : MAINLAND **4 a** : one of the six or seven great divisions of land on the globe **b** *cap* : the continent of Europe — used with *the*

¹con·ti·nen·tal \ˌkän-tᵊn-ˈen-tᵊl\ *adj* (1760) **1 a** : of, relating to, or characteristic of a continent ⟨~ waters⟩; *specif, often cap* : of or relating to the continent of Europe excluding the British Isles **b** *often cap* : of, relating to, or being a cuisine derived from the classic dishes of Europe and esp. France **2 a** *often cap* : of or relating to the colonies later forming the U.S. ⟨*Continental* Congress⟩ **b** : being the part of the U.S. on the No. American continent; *also* : being the part of the U.S. comprising the lower 48 states — **con·ti·nen·tal·ly** \-tᵊl-ē\ *adv*

²continental *n* (1777) **1 a** *often cap* : an American soldier of the Revolution in the Continental army **b** (1) : a piece of Continental paper currency (2) : the least bit ⟨not worth a ~⟩ **2** : an inhabitant of a continent and esp. the continent of Europe

continental breakfast *n, often cap C* (1911) : a light breakfast (as of rolls or toast and coffee)

continental drift *n* (1926) : a hypothetical slow movement of the continents on a deep-seated viscous zone within the earth — compare PLATE TECTONICS

continental shelf *n* (1892) : a shallow submarine plain of varying width forming a border to a continent and typically ending in a steep slope to the oceanic abyss

continental slope *n* (1900) : the usu. steep slope from a continental shelf to the ocean floor

con·tin·gence \kən-ˈtin-jən(t)s\ *n* (ca. 1530) **1** : CONTINGENCY **2** : TANGENCY

con·tin·gen·cy \kən-ˈtin-jən(t)-sē\ *n, pl* **-cies** (1561) **1** : the quality or state of being contingent **2** : a contingent event or condition: as **a** : an event (as an emergency) that may but is not certain to occur ⟨trying to provide for every ~⟩ **b** : something liable to happen as an adjunct to or result of something else *syn* see JUNCTURE

contingency fee *n* (1945) : a fee for services (as of a lawyer) paid upon successful completion of the services and usu. calculated as a percentage of the gain realized for the client — called also *contingent fee*

contingency table *n* (1922) : a table of data in which the row entries tabulate the data according to one variable and the column entries tabulate it according to another variable and which is used esp. in the study of the correlation between variables

¹con·tin·gent \kən-ˈtin-jənt\ *adj* [ME, fr. MF, fr. L *contingent-, contingens*, prp. of *contingere* to have contact with, befall, fr. *com-* + *tangere* to touch — more at TANGENT] (14c) **1** : likely but not certain to happen : POSSIBLE **2** : not logically necessary; *esp* : EMPIRICAL **3 a** : happening by chance or unforeseen causes **b** : subject to chance or unseen effects : UNPREDICTABLE **c** : intended for use in circumstances not completely foreseen **4** : dependent on or conditioned by something else **5** : not necessitated : determined by free choice *syn* see ACCIDENTAL — **con·tin·gent·ly** *adv*

²contingent *n* (1548) **1** : something contingent : CONTINGENCY **2** : a representative group : DELEGATION, DETACHMENT

con·tin·u·al \kən-ˈtin-yü-əl, -yəl\ *adj* [ME, fr. MF, fr. L *continuus* continuous] (14c) **1** : continuing indefinitely in time without interruption ⟨~ fear⟩ **2** : recurring in steady usu. rapid succession ⟨a history of ~ invasions⟩ — **con·tin·u·al·ly** *adv*

syn CONTINUAL, CONTINUOUS, CONSTANT, INCESSANT, PERPETUAL, PERENNIAL mean characterized by continued occurrence or recurrence. CONTINUAL often implies a close prolonged succession or recurrence ⟨*continual* showers the whole weekend⟩. CONTINUOUS usu. implies an uninterrupted flow or spatial extension ⟨football's oldest *continuous* rivalry⟩. CONSTANT implies uniform or persistent occurrence or recurrence ⟨lived in *constant* pain⟩. INCESSANT implies ceaseless or uninterrupted activity ⟨annoyed by the *incessant* quarreling⟩. PERPETUAL suggests unfailing repetition or lasting duration ⟨a land of *perpetual* snowfall⟩. PERENNIAL implies enduring existence often through constant renewal ⟨a *perennial* source of controversy⟩.

con·tin·u·ance \kən-ˈtin-yü-ən(t)s\ *n* (14c) **1** : CONTINUATION **2** : the extent of continuing : DURATION **3** : the quality of enduring : PERMANENCE **4** : an adjournment of a court case to a future day

con·tin·u·ant \-yü-ənt\ *n* (1861) **1** : something that continues or serves as a continuation **2** : a speech sound (as a fricative or vowel) that is produced without a complete closure of the breath passage — compare STOP — **continuant** *adj*

con·tin·u·ate *adj* (1555) *obs* : CONTINUOUS, UNINTERRUPTED

con·tin·u·a·tion \kən-ˌtin-yə-ˈwā-shən\ *n* (14c) **1** : the act or fact of continuing in or the prolongation of a state or activity **2** : resumption after an interruption **3** : something that continues, increases, or adds

con·tin·u·a·tive \kən-ˈtin-yə-ˌwā-tiv, -wə-tiv\ *adj* (1684) : expressing continuity or continuation (as of an idea or action)

con·tin·u·a·tor \-ˌwā-tər\ *n* (1646) : one that continues

con·tin·ue \kən-ˈtin-(ˌ)yü\ *vb* **-tin·ued; -tinu·ing** [ME, fr. MF *continuer*, fr. L *continuare*, fr. *continuus*] *vi* (14c) **1** : to maintain without interruption a condition, course, or action **2** : to remain in existence : ENDURE **3** : to remain in a place or condition : STAY **4** : to resume an activity after interruption ~ *vt* **1 a** : KEEP UP, MAINTAIN ⟨~*s* walking⟩ **b** : to keep going or add to : PROLONG; *also* : to resume after intermission **2** : to cause to continue **3** : to allow to remain in a place or condition : RETAIN **4** : to postpone (a legal proceeding) by a continuance — **con·tinu·er** \-yü-ər\ *n*

syn CONTINUE, LAST, ENDURE, ABIDE, PERSIST mean to exist over a period of time or indefinitely. CONTINUE applies to a process going on without ending ⟨the search for peace will *continue*⟩. LAST, esp. when unqualified, may stress existing beyond what is normal or expected ⟨buy shoes that will *last*⟩. ENDURE adds an implication of resisting destructive forces or agencies ⟨in spite of everything, her faith *endured*⟩. ABIDE implies stable and constant existing esp. as opposed to mutability ⟨a love that *abides* through 40 years of marriage⟩. PERSIST suggests outlasting the normal or appointed time and often connotes obstinacy or doggedness ⟨the sense of guilt *persisted*⟩.

continued *adj* (15c) **1** : lasting or extending without interruption ⟨~ success⟩ **2** : resumed after interruption ⟨a ~ story⟩

continued fraction *n* (ca. 1856) : a fraction whose numerator is an integer and whose denominator is an integer plus a fraction whose numerator is an integer and whose denominator is an integer plus a fraction and so on

continuing *adj* (14c) **1** : CONTINUOUS, CONSTANT ⟨~ poverty⟩ **2** : needing no renewal : ENDURING ⟨~ fame⟩ — **con·tin·u·ing·ly** *adv*

continuing education *n* (1954) : formal courses of study for adult part-time students

con·ti·nu·i·ty \ˌkän-tᵊn-ˈü-ə-tē, -ˈyü-\ *n, pl* **-ties** (15c) **1 a** : uninterrupted connection, succession, or union **b** : uninterrupted duration or continuation esp. without essential change **2** : something that has, exhibits, or provides continuity: as **a** : a script or scenario in the performing arts **b** : transitional spoken or musical matter esp. for a radio or television program **c** : the story and dialogue of a comic strip **3** : the property of being mathematically continuous

con·tin·uo \kən-ˈtin-yə-ˌwō, -ˈti-nə-\ *n, pl* **-u·os** [It, fr. *continuo* continuous, fr. L *continuus*] (1724) : a bass part (as for a keyboard or stringed instrument) used esp. in baroque ensemble music and consisting of a succession of bass notes with figures that indicate the required chords — called also *figured bass, thoroughbass*

con·tin·u·ous \kən-ˈtin-yü-əs\ *adj* [L *continuus*, fr. *continēre* to hold together — more at CONTAIN] (1673) **1** : marked by uninterrupted extension in space, time, or sequence **2** *of a function* : having the property that the absolute value of the numerical difference between the value at a given point and the value at any point in a neighborhood of the given point can be made as close to zero as desired by choosing the neighborhood small enough *syn* see CONTINUAL — **con·tin·u·ous·ly** *adv* — **con·tin·u·ous·ness** *n*

con·tin·u·um \kən-ˈtin-yü-əm\ *n, pl* **-ua** \-yü-ə\ *also* **-u·ums** [L, neut. of *continuus*] (1646) **1** : a coherent whole characterized as a collection, sequence, or progression of values or elements varying by minute degrees ⟨"good" and "bad" . . . stand at opposite ends of a ~ instead of describing the two halves of a line —Wayne Shumaker⟩ **2** : the set of real numbers including both the rationals and the irrationals; *broadly* : a compact set which cannot be separated into two sets neither of which contains a limit point of the other

con·tort \kən-ˈtȯrt\ *vb* [ME, fr. L *contortus*, pp. of *contorquēre*, fr. *com-* + *torquēre* to twist — more at TORTURE] *vt* (15c) : to twist in a violent manner ⟨features ~*ed* with fury⟩ ~ *vi* : to twist into or as if into a strained shape or expression *syn* see DEFORM — **con·tor·tion** \-ˈtȯr-shən\ *n* — **con·tor·tive** \-ˈtȯr-tiv\ *adj*

con·tor·tion·ist \kən-ˈtȯr-sh(ə-)nist\ *n* (1859) : one who contorts; *specif* : an acrobat able to twist the body into unusual postures — **con·tor·tion·is·tic** \-ˌtȯr-shə-ˈnis-tik\ *adj*

¹con·tour \ˈkän-ˌtu̇r\ *n* [F, fr. It *contorno*, fr. *contornare* to round off, fr. ML, to turn around, fr. L *com-* + *tornare* to turn on a lathe — more at TURN] (1662) **1** : an outline esp. of a curving or irregular figure : SHAPE; *also* : the line representing this outline **2** : the general form or structure of something : CHARACTERISTIC — often used in pl. ⟨~*s* of a melody⟩ ⟨to delineate the tortured psychological ~*s* of the tribal past —B. J. Phillips⟩ **3** : a usu. meaningful change in intonation in speech *syn* see OUTLINE

²contour *adj* (1844) **1** : following contour lines or forming furrows or ridges along them ⟨~ flooding⟩ ⟨~ farming⟩ **2** : made to fit the contour of something ⟨a ~ couch⟩ ⟨~ sheets⟩

³contour *vt* (1871) **1 a** : to shape the contour of **b** : to shape so as to fit contours **2** : to construct (as a road) in conformity to a contour

contour feather *n* (1867) : one of the medium-sized feathers that form the general covering of a bird and determine the external contour

contour line *n* (1844) : a line (as on a map) connecting the points on a land surface that have the same elevation

contour map *n* (1862) : a map having contour lines

¹con·tra \ˈkän-trə\ *prep* [L] (15c) **1** : AGAINST — used chiefly in the phrase *pro and contra* **2** : in opposition or contrast to — used before a proper name

EXHIBIT T-2

2 3 0 0 0 3 4 3 3 6

IEEE Std 100-1996

The IEEE Standard Dictionary of Electrical and Electronics Terms

Sixth Edition

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IEEE

The IEEE Standard Dictionary of Electrical and Electronics Terms

Sixth Edition

Standards Coordinating Committee 10, Terms and Definitions
Jane Radatz, Chair

This standard is one of a number of information technology dictionaries being developed by standards organizations accredited by the American National Standards Institute. This dictionary was developed under the sponsorship of voluntary standards organizations, using a consensus-based process.

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9 781559 378338

field-disturbance sensor (measurement procedure for field-disturbance sensors) A device that employs a point source of radio-frequency (rf) energy to detect motion in the vicinity of the source, and in which the emitter and the receiver (or detector) are essentially at the same point, that is, a space-protected system. (EMC) 475-1983r

field-effect transistor A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and source electrodes. (ED) 641-1987w

field emission Electron emission from a surface due directly to high-voltage gradients at the emitting surface. *See also:* electron emission. (ED) [45], 161-1971w

field-enhanced photoelectric emission The increased photoelectric emission resulting from the action of a strong electric field on the emitter. *See also:* phototube. (ED) [45], 161-1971w

field-enhanced secondary emission The increased secondary emission resulting from the action of a strong electric field on the emitter. *See also:* electron emission. (ED) [45], 161-1971w

field excitation current (Hall effect devices) The current producing the magnetic flux density in a Hall multiplier. (MAG) 296-1969w

field-failure protection The effect of a device, operative on the loss of field excitation, to cause and maintain the interruption of power in the motor armature circuit. (IA) [60]

field-failure relay A relay that functions to disconnect the motor armature from the line in the event of loss of field excitation. *See also:* relay. (IA) [60]

field flashing Short-time application of an external direct current source to the field of a synchronous generator to enable it to build up its voltage and become self-excited. (PE) 1020-1988r

field forcing (1) (excitation systems for synchronous machines) A control function that rapidly drives the field current of a synchronous machine in the positive or in the negative direction. (PE) 421.1-1986r
(2) A control function that temporarily overexcites or underexcites the field of a rotating machine to increase the rate of change of flux. *See also:* control. (IA) [60], [75]

field forcing relay A relay that functions to increase the rate of change of field flux by underexciting the field of a rotating machine. *See also:* relay. (IA) [60]

field frame *See:* frame yoke.

field-free emission current (1) (general) The emission current from an emitter when the electric gradient at the surface is zero. (ED) [45], [84]
(2) (cathode) The electron current drawn from the cathode when the electric gradient at the surface of the cathode is zero. *See also:* electron emission. (ED) [45], 161-1971w

field frequency (television) The product of frame frequency multiplied by the number of fields contained in one frequency. *See also:* television. (BT) [34]

field intensity *See:* average detector.

field-intensity meter* A calibrated radio receiver for measuring field intensity. *See also:* interference; interference measurement. (IA) 54-1955w
* Deprecated.

field I^2R loss The product of the measured resistance, in ohms, of the field winding, corrected to a specified temperature, and the square of the field current in amperes. (PE) [84], [9]

field-lead insulation (rotating machinery) The dielectric material applied to insulate the enclosed conductor connecting the collector rings to the coil end windings. *Note:* Field leads also include the pole jumpers forming the series connection between the concentric windings on each pole. Where rectangular strap leads are employed, the insulation may consist of either taped mica and glass or moduled mica and glass or moduled mica and glass composites. Where circular rods are used, moulded laminate tubing is frequently employed as the primary insulation. *See also:* asynchronous machine; direct-current commutating machine. (PE) [9]

field length The number of words or characters in a field. (C) 610.5-1990

field length type An indication of whether the field is fixed or variable in length. *Note:* If a field is a variable length type, the field length expresses the maximum length possible. (C) 610.5-1990

field-limiting adjusting means The effect of a control function or device (such as a resistor) that limits the maximum or minimum field excitation of a motor or generator. *See also:* control. (IA) [60], [75]

field-locking *See:* lock.

field mark A mark that identifies the beginning or the end of a field. (C) 610.10-1994

field measuring instrument A device used to sense and read out the electric or magnetic field intensities surrounding a VDT under test. (For this standard, this instrumentation consists of three parts: probe; readout detector, where the signal from the probe is processed and the data displayed; and any leads between the probe and readout detector.) (EMC) 1140-1994

field mill A device in which a conductor is alternately exposed to the electric field to be measured and then shielded from it. *Note:* The resulting current induced in the conductor is a measure of the electric field strength at the conductor surface. *Synonym:* generating electric field meter. (PE/T&D) 1227-1990r, 539-1990

field molded joint (power cable joints) A joint in which the solid-dielectric joint insulation is fused and curved thermally at the job site. (PE) 404-1986s

field pattern *See:* radiation pattern.

field pole (rotating machinery) A structure of magnetic material on which a field coil may be mounted. *Note:* There are two types of field poles: main and commutating. *See also:* asynchronous machine; direct-current commutating machine. (EEC/PE) [119]

field probe An electrically small field sensor or set of multiple field sensors with various electronics (for example, diodes, resistors, amplifiers, etc.). The output from a field probe cannot be theoretically determined from easily measured physical parameters. (EMC) 1309-1996

field programmable gate array (FPGA) A device containing many circuits whose interconnections and functions are programmable by the user. *Note:* Generally larger than a field programmable logic array. *See also:* dynamically programmable logic gate. (C) 610.10-1994

field programmable logic array (FPLA) A logic array integrated circuit which can be programmed after manufacture, typically at the time of installation. *Note:* The programming is typically done by passing a high current through fusible links on the integrated circuit. *See also:* field programmable gate array; programmable logic array. (C) 610.10-1994

field protection The effect of a control function or device to prevent overheating of the field excitation winding by reducing or interrupting the excitation of the shunt field while the machine is at rest. *See also:* control. (IA) [60], [75]

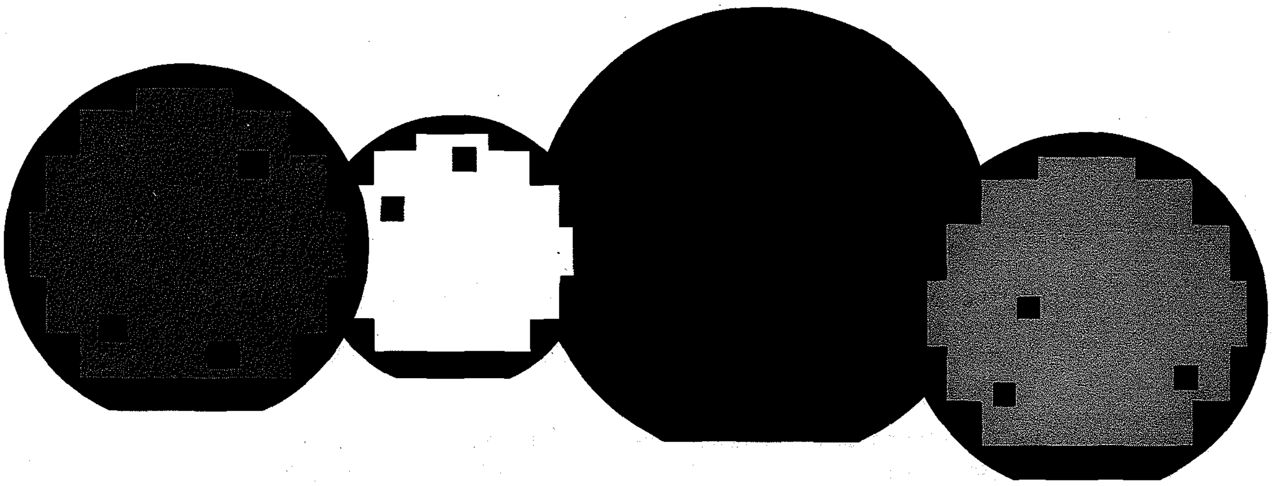
field protective relay A relay that functions to prevent overheating of the field excitation winding by reducing or interrupting the excitation of the shunt field. *See also:* relay. (IA) [60]

field relay (power system device function numbers) A relay that functions on a given or abnormally low value or failure of machine field current, or on an excessive value of the reactive component of armature current in an alternating-current (ac) machine indicating abnormally low field excitation. (PE/SUB) C37.2-1979s

field-reliability test A reliability compliance or determination test made in the field where the operating and environmental conditions are recorded and the degree of control is stated. (R) [29]

EXHIBIT T-3

PRACTICAL INTEGRATED CIRCUIT FABRICATION



Edited by: ICE Staff

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Ultrasonic Bonding	A bonding technique which utilizes ultrasonic energy and pressure to form the bond.
Unipolar	Refers to FET devices where current passes only through one type of semiconductor material (P or N) as it flows from input to output.
Vapor Plating	A vacuum process, usually less than 10^{-10} Torr (mm of Hg), where metal(s) are vaporized through thermal agitation, then recrystallized on cooler surfaces, generally the material to be coated. Also referred to as evaporation.
Via	A path filled with conducting material between circuit layers.
VLSI	**V**ery **L**arge-**S**cale **I**ntegration. ICs that contain 5,000 or more gate equivalents or more than 16,000 bits of memory.
Voltage	Electron potential in an electrical wire or circuit. Usually expressed in volts (V).
Wafer	A thin disk of semiconducting material (usually silicon) on which many separate chips can be fabricated and then cut into individual ICs.
Wedge Bonding	See Bonding, Wedge.
Welding	Joining of two or more pieces of metal by fusing them together.
Working Plates	Masks printed from master plates that are used for production exposure of wafers. As these plates are subject to wear, they must be replaced periodically.
Yellow Room	The room in which wafers are exposed to ultraviolet light in an aligner. Fluorescent lights in the room have yellow filter tubes around them to block unwanted ultraviolet light from that source.
Yield	Yield is the ratio of the number of acceptable units to the maximum number possible.
ZIF Socket	**Z**ero-**I**nsertion **F**orce **S**ocket. A socket in which package leads are readily accepted by the socket, then firmly connected through cam action.

EXHIBIT W-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Hsu et al.	)	Group Art Unit: 2871
Serial No.: 10/921,508	)	Examiner: Nguyen, Thanh Nhan P.
Filed: August 19, 2004	)	Confirmation No. 9818
For: Liquid Crystal Display Cell and Method for Manufacturing the Same	)	TKHR Dkt: 250330-1010 Chi Mei Ref: 92268 US

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

The Office Action dated February 9, 2006, has been carefully considered. In response thereto, please consider the following remarks.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Original) A method for manufacturing a liquid crystal display cell comprising the following steps:

forming a scaling member having a main portion enclosing a display region and a protrusion part extending from the main portion wherein the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member;

dispensing a liquid crystal material upon one of the pair of substrates;

superposing one of the pair of substrates upon the other one such that the liquid crystal material is enclosed by the sealing member;

curing the sealing member;

cutting the pair of substrates to obtain the liquid crystal display cell.

2. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein the sealing material is a radiation-curable adhesive.

3. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein one of the pair of substrates has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

4. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein the cutting step proceeds along a cutting line of the pair of substrates, and the cutting line is across the protrusion part of the sealing member.

5. (Original) A liquid crystal display cell comprising:

a first substrate;

a second substrate;

a liquid crystal layer sandwiched between the first substrate and the second substrate; and

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and a protrusion part extending from the main portion and the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part.

6. (Original) The liquid crystal display cell according to claim 5, wherein the sealing material is a radiation-curable adhesive.

7. (Original) The liquid crystal display cell according to claim 5, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

8. (Original) A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:

a first substrate;

a second substrate;

a liquid crystal layer sandwiched between the first substrate and the second substrate; and

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and a protrusion part extending from the main portion and the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part.

9. (Original) The liquid crystal display device according to claim 8, wherein the sealing material is a radiation-curable adhesive.

10. (Original) The liquid crystal display device according to claim 8, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

11. (Original) A liquid crystal display cell comprising:

a first substrate;

a second substrate;

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and only a protrusion part extending from the main portion; and

a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

12. (Original) The liquid crystal display cell according to claim 11, wherein the main portion has at least four side walls.

13. (Original) The liquid crystal display cell according to claim 12, wherein the main portion is rectangular in shape.

14. (Original) The liquid crystal display cell according to claim 11, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

15. (Original) A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:

a first substrate;

a second substrate;

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and only a protrusion part extending from the main portion; and

a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

16. (Original) The liquid crystal display device according to claim 15, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

17. (Original) The liquid crystal display device according to claim 15, wherein the main portion has at least four side walls.

18. (Original) The liquid crystal display device according to claim 17, wherein the main portion is rectangular in shape.

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed February 9, 2006. Through this response, claims 1-18 remain pending. For at least the following reasons, reconsideration and allowance of the application and pending claims are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 102(e)

A. Statement of the Rejection

Claims 1, 4, 5, 11-13 have been rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by *Choo et al.* ("*Choo*," U.S. Pat. No. 6,822,725). Applicants respectfully traverse this rejection.

B. Discussion of the Rejection

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e).

In the present case, not every feature of the claimed invention is represented in the *Choo* reference. Applicants discuss the *Choo* reference and Applicants' claims in the following. Claim 1 recites:

1. A method for manufacturing a liquid crystal display cell comprising the following steps:

> **forming a sealing member *having* a *main portion* *enclosing* *a display region* and a protrusion part extending from the main portion** wherein the sealing member is formed by the following steps:
>
> applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and
>
> continuing applying the sealing material along the display region to form the main portion of the sealing member;
>
> dispensing a liquid crystal material upon one of the pair of substrates;
>
> superposing one of the pair of substrates upon the other one such that the liquid crystal material is enclosed by the sealing member;
>
> curing the sealing member;
>
> cutting the pair of substrates to obtain the liquid crystal display cell.

(*Emphasis Added*).

The Office Action alleges that *Choo* discloses forming a sealing member having a main portion enclosing a display region by pointing to reference numeral 36 of FIG. 6 of the *Choo* reference. Applicants respectfully submit that the reference does not disclose forming a sealing member ***enclosing*** a display region. As can be seen with reference to FIG. 6 of *Choo*, the depicted seal line forms a liquid crystal introducing inlet 37, and clearly ***does not enclose*** the display region of the depicted LCD module. Quite the opposite, the depicted LCD module is explicitly shown with a liquid crystal introducing inlet 37 that provides an opening into the display region of the LCD module. *See Choo*, col. 6, lines 61-67.

In contrast to the cited reference, the claimed invention, as highlighted above in independent claim 1, discloses forming a sealing member that ***encloses*** a display region of a liquid crystal display cell. This feature is further depicted in FIG. 4 of the present application, where it should be appreciated that the sealing member 110 has a main portion 110a ***enclosing the display region*** 122 and a protrusion part 110b extending from the main portion 110a wherein the liquid crystal layer 106 is formed within the display region 122 ***enclosed by the main portion*** 110a. The Specification, pg. 5, lines 1-7.

Further, in contrast to the claimed invention, the cited *Choo* reference pertains to a process of fabricating LCD panels relying on injection of liquid crystal material into a liquid crystal introducing inlet 37, and not to the more advanced one drop fill (ODF) method discussed in the instant application. The ODF fabrication method does not rely on the injection of liquid crystal material through a liquid crystal introducing inlet, which may require forming a sealing member that does not enclose the display region of an LCD cell. As noted above, the claimed invention discloses forming a sealing member having a main portion ***enclosing*** a display region.

Accordingly, Applicants submit that for at least the above discussed reasons, indepenent claim 1 is allowable over the *Choo* reference because the cited reference does not disclose, teach or suggest all elements of the claimed invention. Because independent claim 1 is allowable over *Choo*, dependent claims 2-4 are allowable as a matter of law for at least the reason that the dependent claims 2-4 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

With regard to independent claim 5, Applicants submit that claim is allowable for at least the reasons discussed above in reference to independent claim 1. Claim 5 recites:

> 5. A liquid crystal display cell comprising:
> a first substrate;
> a second substrate;
> a liquid crystal layer sandwiched between the first substrate and the second substrate; and
> a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, ***wherein the sealing member has a main portion enclosing a display region*** and a protrusion part extending from the main portion and the sealing member is formed by the following steps:
> applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and
> continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part.

(*Emphasis added*). As noted above in reference to independent claim 1, the cited reference does not disclose, teach or suggest at least the above highlighted elements of independent claim 5. Accordingly, Applicants respectfully submit that independent claim 5 is allowable over *Choo*. Further, Applicants submit that dependent claims 6-7 are allowable as a matter of law for at least the reason that the dependent claims 6-7 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

With regard to independent claim 11, Applicants submit that claim is allowable for at least the reasons discussed above in reference to independent claim 1. Claim 11 recites:

> 11. A liquid crystal display cell comprising:
> a first substrate;
> a second substrate;
> a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, ***wherein the sealing member has a main portion <u>enclosing</u> a display region*** and only a protrusion part extending from the main portion; and
> a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

(*Emphasis added*). As noted above in reference to independent claim 1, the cited reference does not disclose, teach or suggest at least the above highlighted elements of independent claim 11. Accordingly, Applicants respectfully submit that independent claim 11 is allowable over *Choo*. Further, Applicants submit that dependent claims 12-14 are allowable as a matter of law for at least the reason that the dependent claims 12-14 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Due to the shortcomings of the *Choo* reference described in the foregoing, Applicants respectfully assert that *Choo* does not anticipate Applicants' claims. Therefore, Applicants respectfully request that the rejection of these claims be withdrawn.

II. Claim Rejections - 35 U.S.C. § 103(a)

A. Rejection of Claims

Claims 2, 3, 6, 7 and 14 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Choo* in view of *Admission* ("*Prior Art*"). Claims 8-10 and 15-18 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Choo* in view of *Admission* and further in view of *Suzuki* ("*Suzuki*," U.S. Pub. No. 2002/0012094). Applicants respectfully traverse this rejection.

B. Discussion of the Rejection

With regard to dependent claims 2, 3, 6, 7, and 14, Applicants submit that these claims are allowable as a matter of law because they contain all limitations of their respective allowable base claims, as noted above.

As has been acknowledged by the Court of Appeals for the Federal Circuit, the U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness by showing some objective teaching in the prior art or generally available knowledge of one of ordinary skill in the art that would lead that individual to the claimed invention. *See In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Manual of Patent Examining Procedure (MPEP) section 2143 discusses the requirements of a *prima facie* case for obviousness. That section provides as follows:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or

references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must be found in the prior art, and not based on applicant's disclosure.

In the present case, the *Choo* in view of *Suzuki* fails to disclose, teach or suggest all elements of the claimed invention. In particular, claim 8 recites:

8. A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:
a first substrate;
a second substrate;
a liquid crystal layer sandwiched between the first substrate and the second substrate; and
a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, ***wherein the sealing member has a main portion <u>enclosing</u> a display region*** and a protrusion part extending from the main portion and the sealing member is formed by the following steps:
applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and
continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part.

(*Emphasis added*). As noted above in reference to independent claim 1, the cited reference does not disclose, teach or suggest at least the above highlighted elements of independent claim 8. Accordingly, Applicants respectfully submit that independent claim 8 is allowable over *Choo* in view of *Suzuki*. Further, Applicants submit that dependent claims 9-10 are allowable as a matter of law for at least the reason that the dependent claims 9-10 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Claim 15 recites:

15. A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:
a first substrate;
a second substrate;

> a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, ***wherein the sealing member has a main portion <u>enclosing</u> a display region*** and only a protrusion part extending from the main portion; and
>
> a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

(*Emphasis added*). As noted above in reference to independent claim 1, the cited reference does not disclose, teach or suggest at least the above highlighted elements of independent claim 15. Accordingly, Applicants respectfully submit that independent claim 15 is allowable over *Choo* in view of *Suzuki*. Further, Applicants submit that dependent claims 16-18 are allowable as a matter of law for at least the reason that the dependent claims 16-18 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

In summary, it is Applicants' position that a *prima facie* for obviousness has not been made against Applicants' claims. Therefore, it is respectfully submitted that each of these claims is patentable over the cited references and that the rejection of these claims should be withdrawn.

As a separate and independent basis for the patentability of the claims rejected under 35 U.S.C. §103(a), Applicants respectfully traverse the rejections as failing to identify a proper basis for combining the cited references. In combining these references, the Office Action failed to allege ANY motivation for combining the cited reference with Applicants' admitted prior art. Consequently, this embodies a legally rejection, in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching <u>in the prior art</u> to suggest to one skilled in the art that the claimed invention would have been obvious. <u>W. L. Gore & Associates, Inc. v. Garlock</u>

Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a liquid crystal display cell, as claimed by the Applicants.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50

USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

CONCLUSION

It is not believed that any fees are required, beyond those which may otherwise be provided for in the documents accompanying this paper. However, in the event that additional fees are necessary, such fees are hereby authorized to be charged to Deposit Account No. 20-0778.

Respectfully submitted,

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EXHIBIT W-3

US006822725B2

(12) **United States Patent**
Choo et al.

(10) **Patent No.: US 6,822,725 B2**
(45) **Date of Patent: Nov. 23, 2004**

(54) **LIQUID CRYSTAL DISPLAY SUBSTRATES INTEGRATED BY SEALANT FORMED INSIDE CUTTING LINES**

(75) Inventors: **Dae-ho Choo**, Suwon (KR); **Byeong-ill Kim**, Seoul (KR); **Sung-uk Jung**, Seoul (KR); **Woo-shik Lee**, Seoul (KR); **Bum-soo Kim**, Suwon (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/461,412**

(22) Filed: **Jun. 16, 2003**

(65) **Prior Publication Data**

US 2003/0206266 A1 Nov. 6, 2003

Related U.S. Application Data

(60) Continuation of application No. 09/920,799, filed on Aug. 3, 2001, now Pat. No. 6,580,489, which is a division of application No. 09/231,109, filed on Jan. 14, 1999, now Pat. No. 6,297,869.

(30) **Foreign Application Priority Data**

Dec. 4, 1998 (KR) 1998-53540
Dec. 4, 1998 (KR) 1998-53543
Dec. 4, 1998 (KR) 1998-53548

(51) **Int. Cl.**[7] **G02F 1/13**; G02F 1/1339

(52) **U.S. Cl.** **349/187**; 349/153; 349/190

(58) **Field of Search** 349/153, 187, 349/189, 190

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Primary Examiner—Tarifur R. Chowdhury
(74) *Attorney, Agent, or Firm*—McGuireWoods LLP

(57) **ABSTRACT**

Disclosed is a liquid crystal display panel capable of being cut by a laser light. The liquid crystal display panel according to the present invention includes a substrate having a buffer layer between a conducting layer and an inner surface of the substrate, in which the buffer layer is disposed along a cutting line and spreads a crack and edges of the conducting layer is positioned in a region defined by the cutting line. Further, a method for manufacturing the liquid crystal display panel is disclosed, in which the liquid crystal display panel is machined by a laser cutter and a laser grinder.

13 Claims, 11 Drawing Sheets

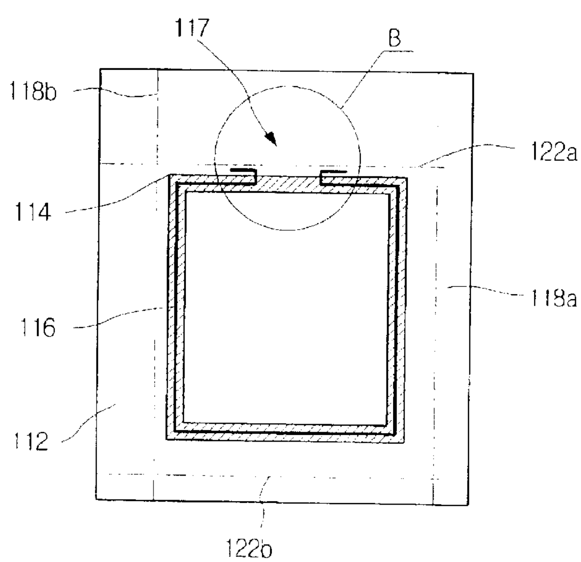


FIG. 1
(PRIOR ART)

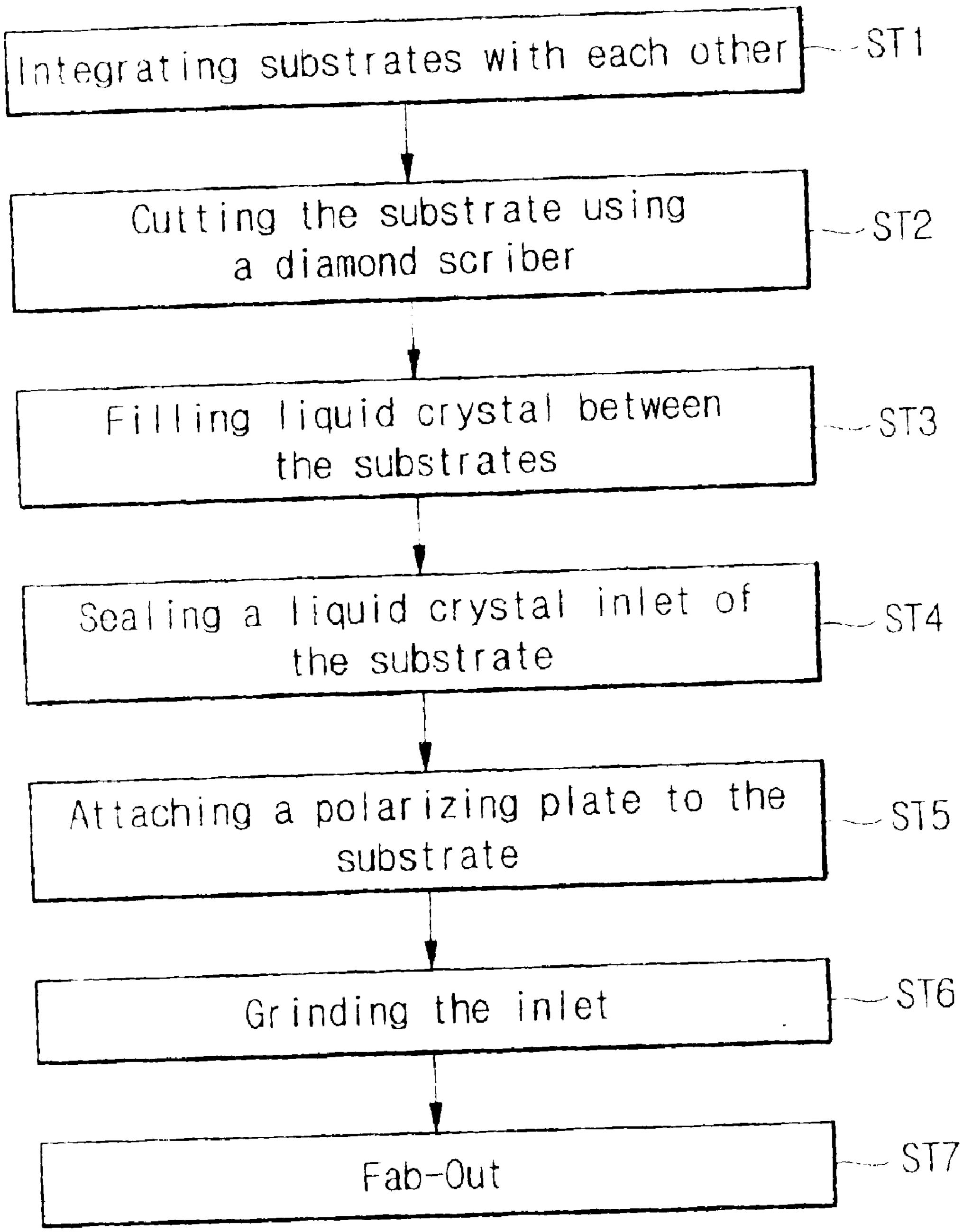


FIG. 2
(PRIOR ART)

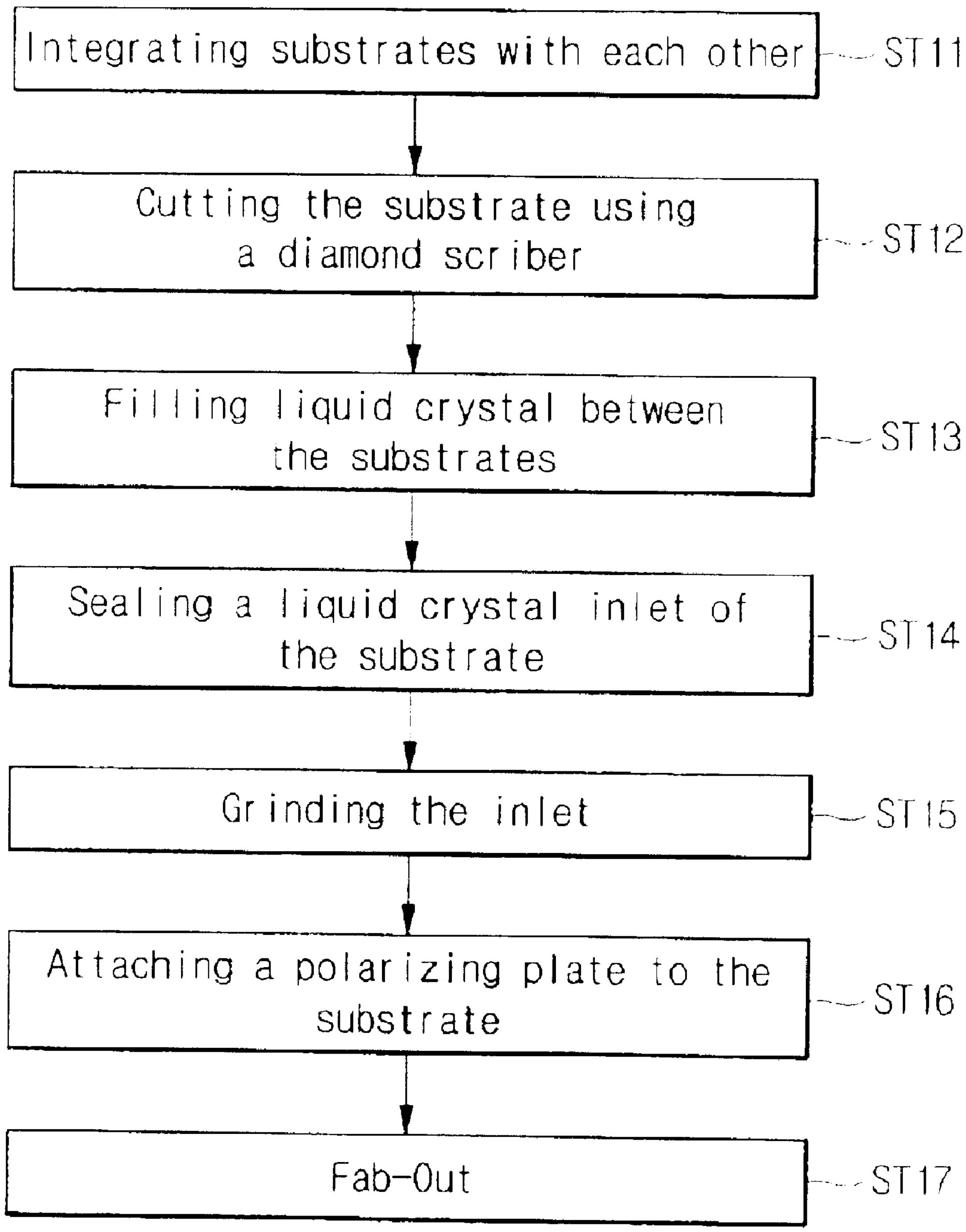


FIG. 3
(PRIOR ART)

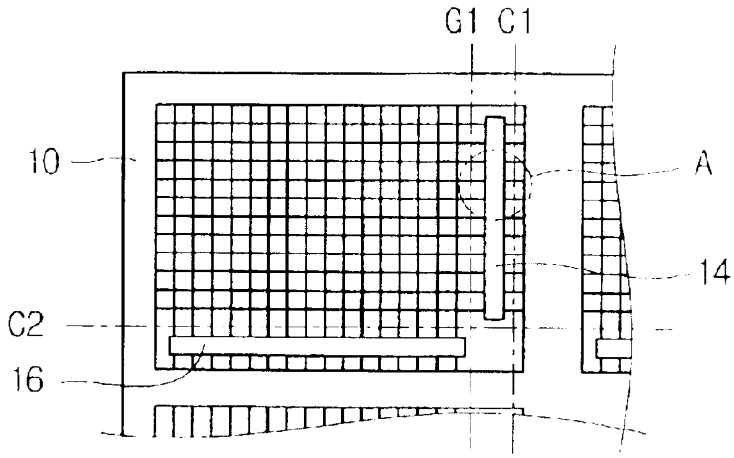


FIG. 4
(PRIOR ART)

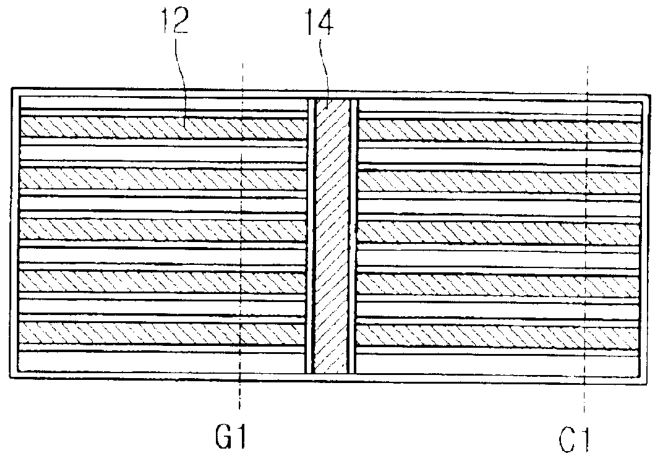


FIG. 5A
(PRIOR ART)

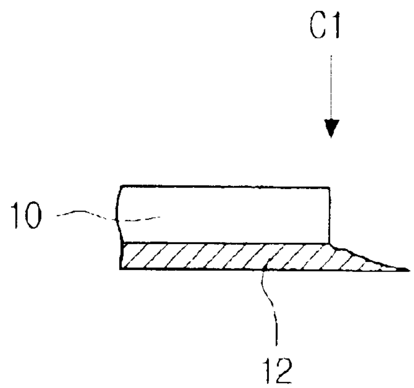


FIG. 5B
(PRIOR ART)

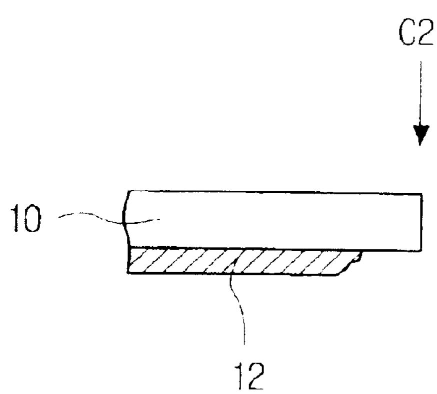


FIG. 6

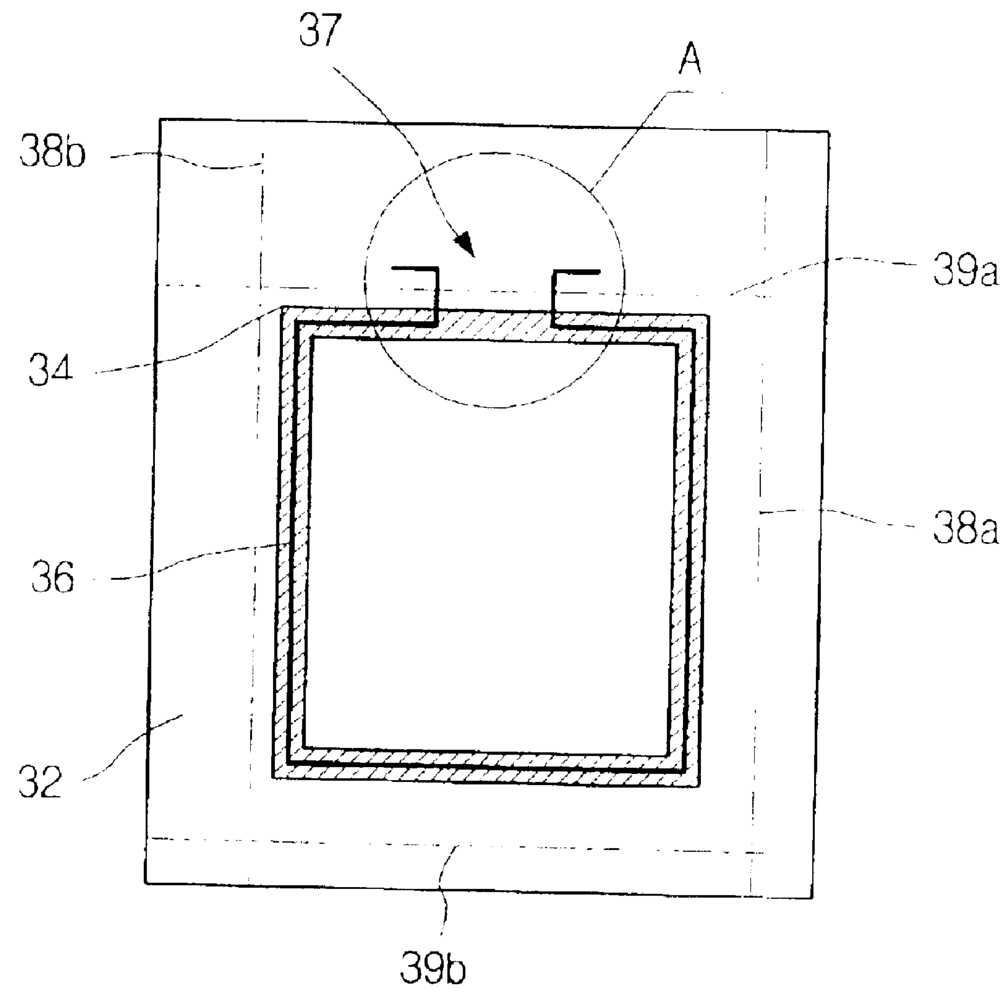


FIG. 7

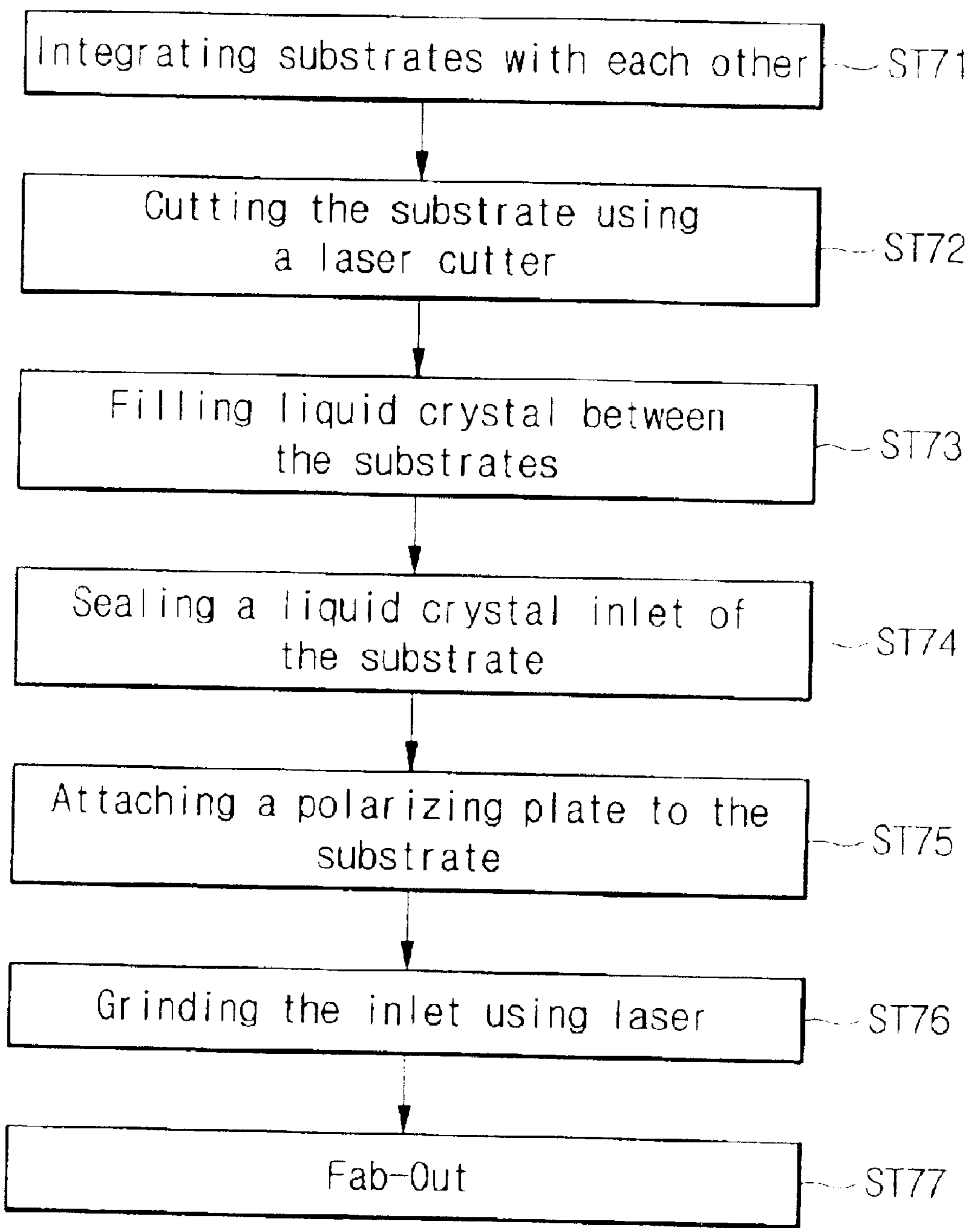

Integrating substrates with each other
ST71
Cutting the substrate using a laser cutter
ST72
Filling liquid crystal between the substrates
ST73
Sealing a liquid crystal inlet of the substrate
ST74
Attaching a polarizing plate to the substrate
ST75
Grinding the inlet using laser
ST76
Fab-Out
ST77

FIG. 8

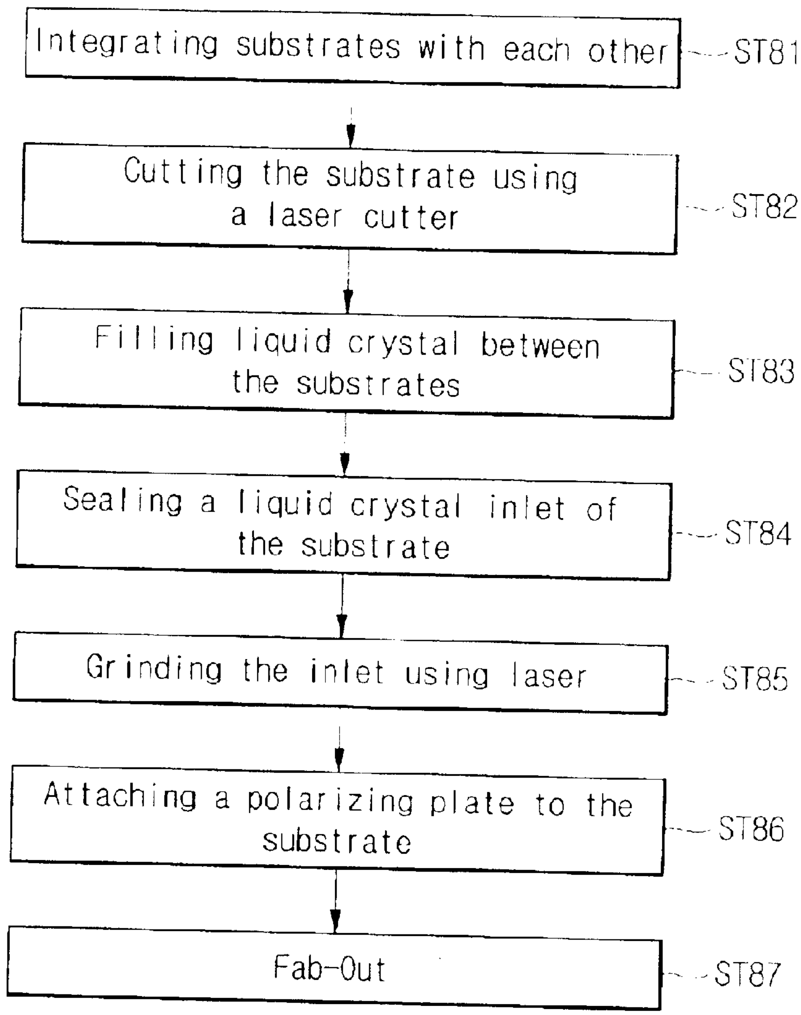
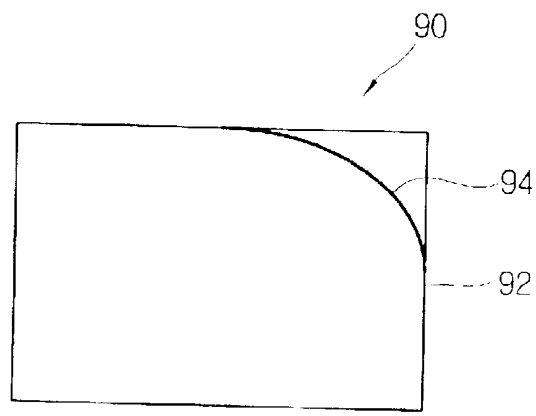

Integrating substrates with each other
ST81
Cutting the substrate using a laser cutter
ST82
Filling liquid crystal between the substrates
ST83
Sealing a liquid crystal inlet of the substrate
ST84
Grinding the inlet using laser
ST85
Attaching a polarizing plate to the substrate
ST86
Fab-Out
ST87

FIG. 9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94
92

FIG. 10

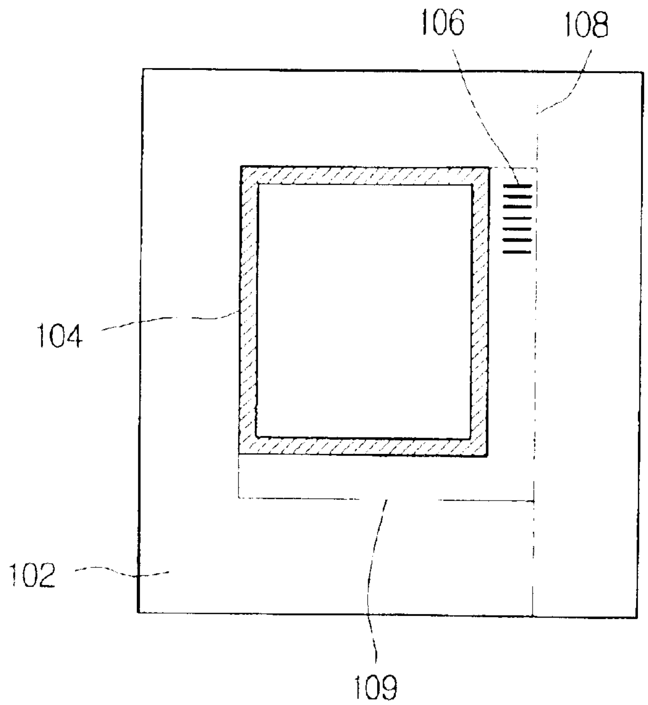


FIG. 11

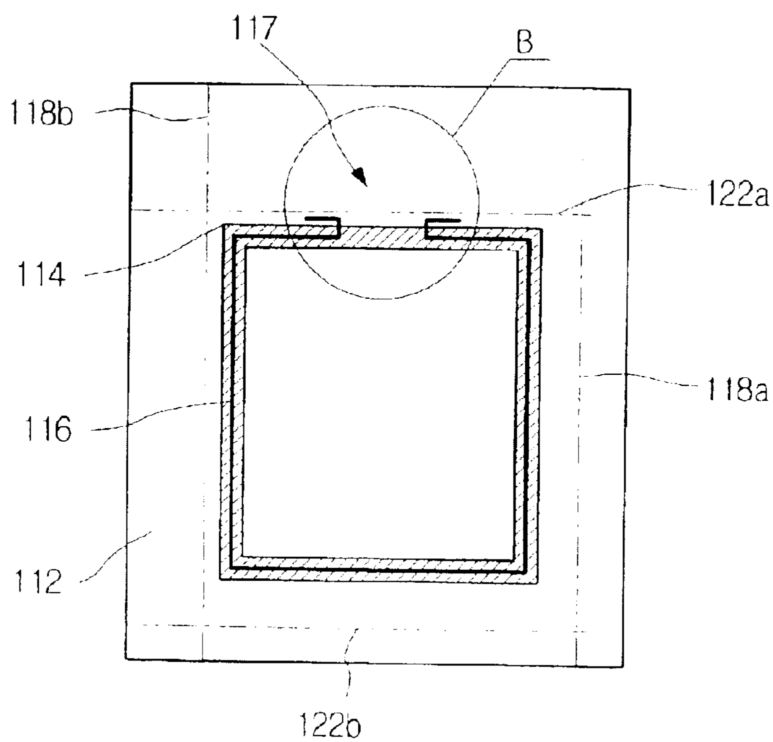


FIG. 12

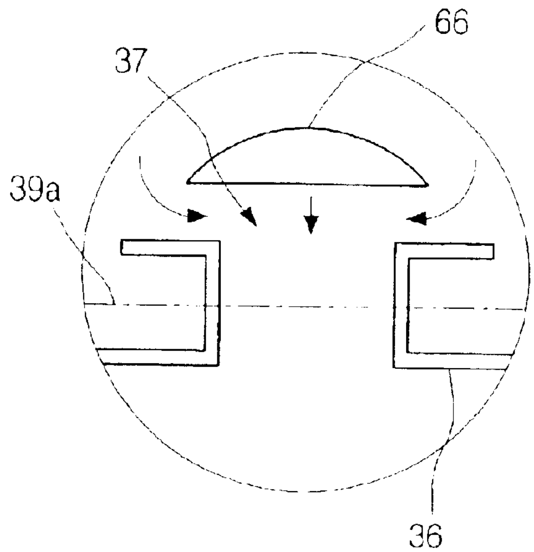


FIG. 13

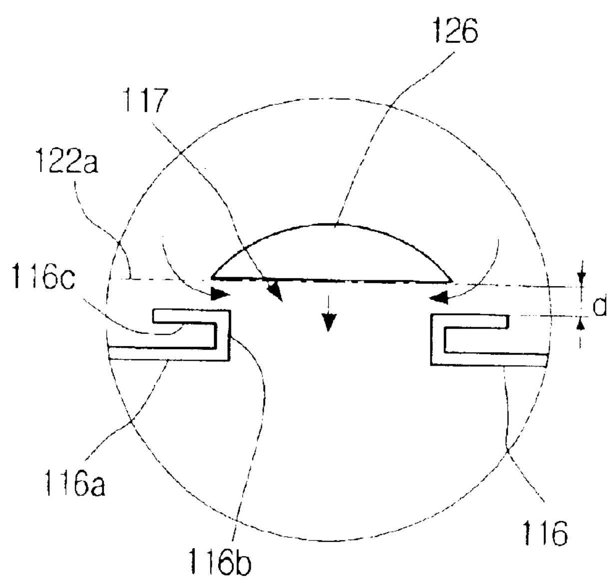


FIG. 14

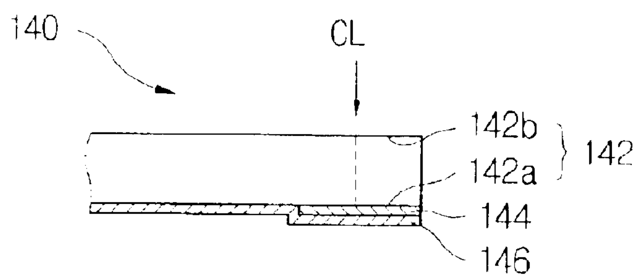


FIG. 15

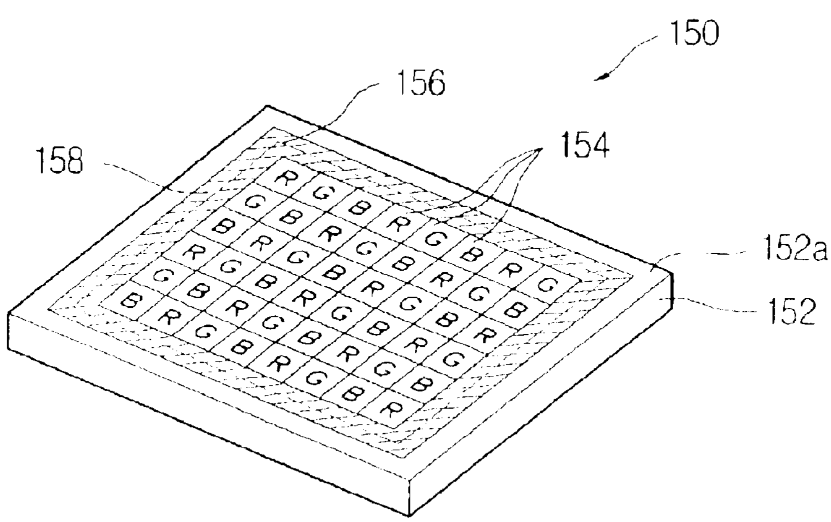


FIG. 16

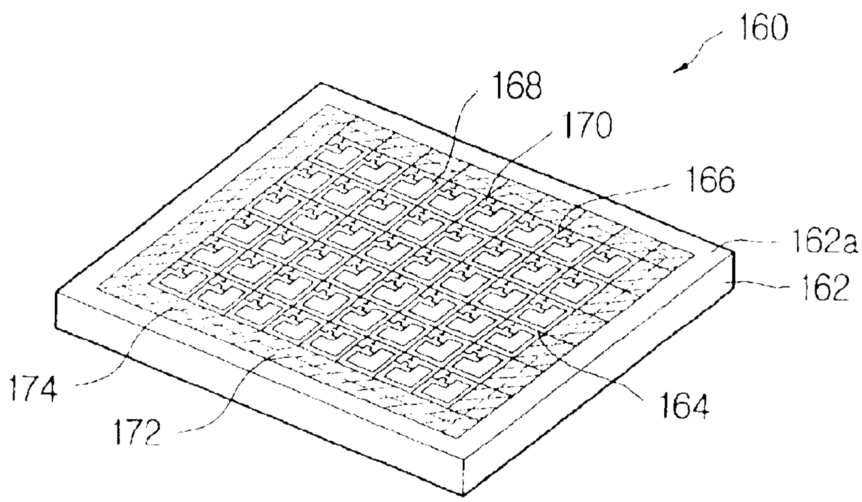
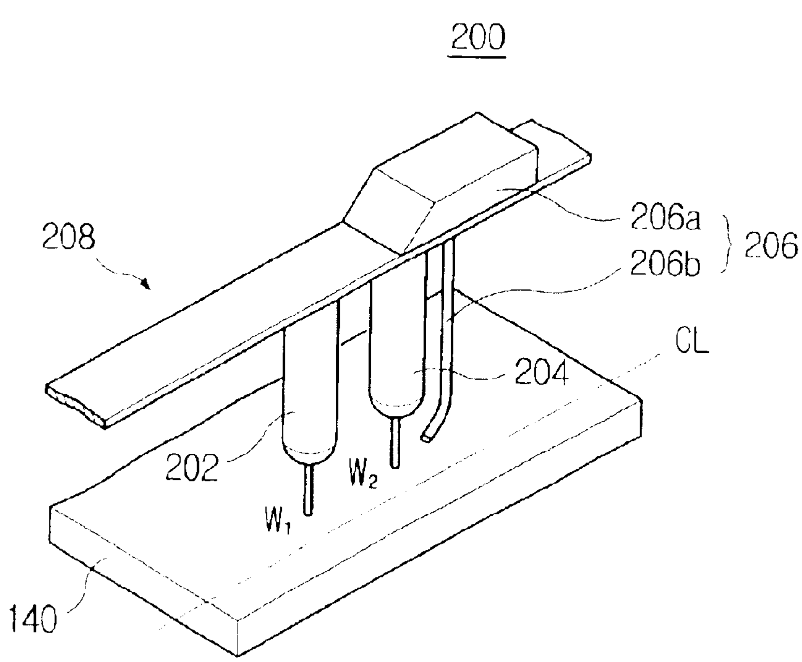

160
168
170
166
162a
162
164
174
172

FIG. 17


200
208
206a
206b
206
CL
204
202
W_2
W_1
140

LIQUID CRYSTAL DISPLAY SUBSTRATES INTEGRATED BY SEALANT FORMED INSIDE CUTTING LINES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is continuation of U.S. patent application Ser. No. 09/920,799 filed on Aug. 3, 2001, which has now become U.S. Pat. No. 6,580,489, which is a divisional of the U.S. patent application Ser. No. 09/231,109 filed on Jan. 14, 1999, which has now become U.S. Pat. No. 6,297,869.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display panel, and more particularly to a structure of an upper and lower substrates of the liquid crystal display panel which is cut into an unit panel before a liquid crystal is introduced between the upper and lower substrates integrated with each other. Further, the present invention relates to a manufacturing the liquid crystal display panel which is capable of being cut by a laser light.

2. Description of the Prior Art

Recently, a liquid crystal display (hereinafter, referred to as a LCD) module is widely used as a display unit instead of a cathode ray tube, because of its small size, light weight, and low consumption of power. The LCD module is a plan display unit using a liquid crystal as a light shutter transmitting and screening a transmission of the light, according to the electric signal.

A thin film transistor LCD module (hereinafter, referred to as TFT LCD module) is provided with a TFT substrate, a color filter substrate, and a liquid crystal introduced between the TFT substrate and the color filter substrate. The TFT substrate and the color filter substrate are made of two parent glass substrates which are respectively divided into six LCD panels.

The parent glass substrate which is used for the TFT substrate has a plurality of gate lines, a plurality of data lines which are respectively intersected with each gate line, TFT devices respectively formed at each intersection of the gate lines and the data lines, and pixel electrodes.

Another parent glass substrate which is used for the color filter substrate includes color filter layers respectively having red, green, and blue, a black matrix, and corresponding electrodes. The black matrix prevents a mixture of light in the color filter layers and keeps the thin film transistors from operating in an off-state.

The TFT substrate and the color filter substrate as constructed above are arranged, assembled together and cut along a cutting line into a plurality of the LCD panels before the liquid crystal is introduced between the substrates.

FIGS. **1** and **2** are views showing processes of cutting the integrated substrate by using a diamond scriber and attaching a polarizing plate to the substrate.

Referring to FIG. **1**, a method of manufacturing an LCD panel according to the conventional art includes a step ST**1** of integrating substrates, a step ST**2** of cutting the integrated parent substrates using the diamond scriber, a step ST**3** of filling the liquid crystal between the integrated substrates, a step ST**4** of sealing a liquid crystal introducing inlet of the integrated substrates, a step ST**5** of attaching the polarizing plates to outer surfaces of the integrated substrates, a step ST**6** of grinding a cut surface of the substrates using a grinder, and a step ST**7** of transferring the substrates to an assembling stage.

Referring to FIG. **2**, a method of manufacturing an LCD panel according to another conventional art includes a step of cutting the integrated parent substrates using a diamond scriber, a step of filling the liquid crystal between the integrated substrates, a step of sealing a liquid crystal introducing inlet of the integrated substrates, a step of grinding a cut surface of the substrates using a grinder, a step of attaching the polarizing plates to outer surfaces of the integrated substrates, and a step ST**7** of transferring the substrates to an assembling stage.

Regarding methods of manufacturing the LCD panel according to the conventional art, at the grinding step, one of the integrated substrates is cut along cutting lines C**1**, C**2** and G**1**, and then has been grinded at a predetermined angle at the corner of cut surfaces thereof, as shown in FIGS. **3** and **4**. In FIGS. **3** and **4**, a reference numeral **14** denotes a short bar connecting gate lines **12** with each other and a reference numeral **16** indicates a short bar connecting data lines with each other. The short bars **14** and **16** discharge the static electricity generated while cutting the substrates.

The grinding step removes glass chips remaining at edges of the substrates from the substrates, prevents damage to a printed circuit board attached to a pad and protects the gate line, the data lines and the panel from cracking.

According to the method referred in FIG. **1**, the glass chips around the edges of the substrates generated during the cutting step cause defects in attaching the polarizing plates to the substrates. The defect in the attachment of the polarizing plates forces the polarizing plates to be re-attached, which increases a manufacturing cost.

The method in which the substrate is ground before attaching the polarizing plates as referred in FIG. **2** may remarkably reduce defects in the polarizing plate attachment. However, the removal of the short bar **14** from the substrates cut along the cutting line G**1** as shown in FIGS. **3** and **4**, causes malfunction of the panel's TFTs due to the static charges due to a friction during the grinding step.

Referring to FIG. **3** again, the cutting of the parent substrate using the laser light starts at an outer surface of the substrate. The parent glass substrate can be cut along the cutting lines, but the interconnection lines **12** formed on an inner surface of the substrate are occasionally not cut. As shown in FIGS. **5***a* and **5***b*, even though the parent glass substrate **10** is exactly cut along the cutting lines C**1** and C**2**, the crack generated in the parent glass substrate **10** may not be transferred to the interconnection lines **12** disposed on the inner surface of the substrate and the interconnection lines **12** are not exactly cut.

It is considered that the cutting problems are caused by the ductility and heat expansion difference of metals used for the interconnection lines.

Sealant is coated on the inner surface of one substrate in order to integrate the substrates together.

FIG. **6** is a view showing the sealant coated on the substrate, the liquid crystal introducing inlet **37**, and the cutting line **39***a* on the substrate according to the present invention. Reference numerals **38***a*, **38***b*, **39***a*, and **39***b* respectively denote the cutting line and reference numeral **34** indicates the black matrix.

Referring to FIG. **6**, a seal line formed on the substrate, except for the liquid crystal introducing inlet is not overlapped with the cutting line. However, a part of the seal line forming the liquid crystal introducing inlet extends across the cutting line **39***a*. Therefore, since the cutting line **39***a* near the liquid crystal introducing inlet **37** is cut under a cutting condition different from another cutting lines, it is

difficult to cut the integrated substrate into a plurality of panels by laser. Thus, different cutting conditions for the portion near the liquid crystal introducing inlet and for the rest of the substrate have to be set up, which complicates the cutting process.

As shown in FIG. **12**, in the case that the cutting line **39***a* extends across a neck portion of the liquid crystal introducing inlet **37**, there is a problem in that when the sealant **56** is supplied to close the liquid crystal introducing inlet **37**, air is introduced through the liquid crystal introducing inlet **37** into a liquid crystal layer between the integrated substrate **32**.

SUMMARY OF THE INVENTION

The present invention has been made to overcome the above described problems of the prior art.

It is an object of the present invention to provide a substrate for a liquid crystal display panel, in which glass chips are prevented from being created during a cutting of the substrate.

It is another object of the present invention to provide a liquid crystal display panel of which substrates are grinded without generating static charges.

It is still an object of the present invention to provide a method of manufacturing a liquid crystal display panel capable of being cut by a laser light, in which a conducting layer formed in an inner surface of a substrate can be prevented from being cut during the cutting of the substrate.

It is still further an object of the present invention to provide a method of manufacturing a liquid crystal display panel capable of being cut by a laser light, in which air can be prevented from being introduced through a liquid crystal inlet between the substrates of the panel at a step of sealing the liquid crystal inlet.

To accomplish the above object of the present invention, according to an aspect of the present invention, there is provided a method of manufacturing a liquid crystal display panel capable of being cut by laser, comprising the steps of:

emitting a laser light to cut a substrate along a cutting line indicated on the substrate; and

attaching a polarizing plate to an outer surface of the substrate.

The method of manufacturing a liquid crystal display panel capable of being cut by laser further comprising a step of grinding edges of a cut surface of the substrate after the step of attaching the polarizing plate to the outer surface of the substrate.

The step of grinding the edges of the cut surface of the substrate may be performed after the step of attaching the polarizing plate to the outer surface of the substrate.

The laser light focused on the substrate has an ellipse shape, of which an apsis line is parallel to the cutting line and a minor line is normal to the cutting line. Therefore, the grinding using the laser light can be omitted.

A parent substrate for the liquid crystal display panel according to the present invention includes a short bar thereon connecting the wire with the others and has the first and second cutting lines which is spaced at a predetermined distance from and parallel to both side of the short bar.

According to another aspect of the present invention, there is provided a method of manufacturing a liquid crystal display panel capable of being cut by laser, comprising the steps of:

cutting a panel along a cutting line using laser, the panel being formed in such a manner that a first transparent insulated substrate having a thin film transistor and wires and pixel electrodes connected with the thin film transistor on an inner surface thereof is integrated to face a second transparent insulated substrate having a color filter layer and electrodes on an inner surface thereof;

introducing liquid crystal in a space between the first and second transparent substrates and sealing an inlet for introducing the liquid crystal;

grinding edges of the first and second cut substrates using laser; and

attaching polarizing plates to each of outer surfaces of the first and second substrates.

According to still another aspect of the present invention, there is provided a liquid crystal display panel capable of being cut by laser, comprising:

a first transparent insulated substrate having a thin film transistor and wires and pixel electrodes connected with the thin film transistor on an inner surface thereof, ends of the wires are positioned at a predetermined position near a cutting line on the first transparent insulated substrate;

a second transparent insulated substrate having a color filtering layer and electrodes corresponding to the pixel electrodes on an inner surface thereof; and

sealant which is disposed along edges of one of the first and second substrates to form an inlet for introducing the liquid crystal in a place in order that the first transparent insulated substrate is integrated with the second transparent insulated substrate,

wherein the panel is cut along the cutting line.

According to still further aspect of the present intention, there is provided a substrate capable of being cut by laser comprising:

a substrate having an inner surface and an outer surface with a cutting line;

a conducting layer which is deposited on the inner surface along a cutting line of the inner surface corresponding to the cutting line on the outer surface of the substrate; and

a buffer layer which is disposed along the cutting line between the inner surface and the conducting layer of the substrate,

wherein the substrate and the buffer layer are separately cut by laser having different wavelength and the buffer layer is cracked by the conducting layer.

According to still further aspect of the present invention, there is provided a liquid crystal display panel capable of being cut by laser comprising:

a first transparent insulating substrate including thin film transistors formed on an inner surface and a wire connected with the thin film transistors and pixel electrodes;

a second transparent insulating substrate having an inner surface corresponding to the first transparent insulating substrate, a color filter layer formed on the inner surface, a black matrix and corresponding electrodes; and

a buffer layer which is disposed between the conducting layer and the inner surface and diffuses a crack generated therein to the conducting layer vertically,

wherein one of the first and second substrate has a cutting line on an outer surface thereof and the first and second substrates and the buffer layer are respectively cut by laser having a different wavelength.

The first and second transparent insulating substrates is made of a parent glass substrate which has an area corresponding to a sum of areas of the first and second substrates.

The buffer layer is formed on the inner surface of one of the first and second substrates along a cutting line corresponding to the cutting line formed on the outer surface of one of the first and second substrates, with a predetermined width.

The buffer layer is formed on the inner surfaces of the first and second transparent insulating substrates along cutting lines corresponding to the cutting line on the outer surface, with a predetermined width.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and other advantages of the present invention will become more apparent by describing in detail the preferred embodiment thereof with reference to the attached drawings, in which:

FIGS. **1** and **2** respectively are flow charts showing a process of manufacturing a liquid crystal display panel according to the conventional art;

FIG. **3** is a schematic plan view of a thin film transistor substrate of the liquid crystal display panel according to the conventional art;

FIG. **4** is a detailed view of the thin film transistor substrate, marked in a circle A in FIG. **3**;

FIGS. **5***a* and **5***b* are partially sectional views of the thin film transistor substrate, in which FIG. **5***a* is a sectional view of the thin film transistor substrate, taken along a line C**1** and FIG. **5***b* is a sectional view of the thin film transistor substrate, taken along a line C**2** in FIG. **3**;

FIG. **6** is a plan view of a liquid crystal display panel according to an embodiment of the present invention;

FIGS. **7** and **8** are flow charts showing a process of manufacturing the liquid crystal display panel according to the embodiment of the present invention;

FIG. **9** is a partially sectional view of a corner of the substrate for the liquid crystal display panel according to the present invention, in which the corner of the substrate is grinded;

FIG. **10** is a schematic plan view of a liquid crystal display panel according to another embodiment of the present invention;

FIG. **11** is a schematic plan view of a liquid crystal display panel according to still another embodiment of the present invention;

FIG. **12** is an enlarged view of a portion marked in a circle A in FIG. **6**;

FIG. **13** is an enlarged view of a portion marked in a circle B in FIG. **11**;

FIG. **14** is a partial sectional view of a substrate to be cut according to still another embodiment of the present invention;

FIG. **15** is a perspective view of a color filter substrate to be cut according to still another embodiment of the present invention;

FIG. **16** is a perspective view of a thin film transistor substrate to be cut according to still another embodiment of the present invention; and

FIG. **17** is a schematic perspective view of a laser cutter for cutting substrates in FIGS. **14** to **16**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, a method of manufacturing a liquid crystal display panel capable of being cut by a laser light and a substrate for the liquid crystal display panel according to the present invention will be described in detail with reference to accompanying drawings.

Embodiment 1

FIGS. **7** and **8** are flow charts showing a process of manufacturing a liquid crystal display panel according to the embodiment of the present invention.

Referring to FIG. **7**, an integrated substrate is provided at a step ST**71**. The integrated substrate is comprised of a parent glass substrate for a thin film transistor substrate (hereinafter, referred to as TFT substrate) having an area corresponding to an area of at least one panel and a parent glass substrate for a color filer.

The parent glass substrate for the TFT substrate includes a plurality of gate lines, a plurality of data lines formed to intersect with the gate lines, thin film transistors and pixel electrodes formed at a point that the data lines intersects with the gate lines.

The parent glass substrate also has short bars **14** disposed at each end of interconnection lines to be normal to the interconnection lines, connecting the interconnection lines with each other to prevent static charges from damaging TFTs on the panel while cutting, as shown in FIGS. **3** and **4**. Cutting lines C**1** and C**2** locates parallel to and apart from the short bar **14** at a predetermined distance.

The parent glass substrate for the color filter substrate has formed thereon color filter layers respectively provided with red, green, and blue, a black matrix, and corresponding electrodes. The black matrix prevents lights of the color filter layers from being mixed and also prevents the TFTs from operating in an off line state.

The integrated substrate is cut along the cutting line by laser, at step ST**72**. The integrated substrates are cut by laser light one substrate and then the other substrate. The selected substrate is cut from the outer surface to the inner surface.

The substrate has a smooth cut surface, unlike a surface of the substrate cut by a diamond blade. Further, glass chips are not generated while grinding the substrate. Accordingly, it is possible to minimize errors due to the glass chips when attaching the polarizing plate to the outer surface of the substrate. The interconnection lines are cut sometimes because the glass chips press the interconnection lines during a process of TCP bonding. However, few glass chips generated while cutting the substrate prevent the interconnection lines from being cut during the process of TCP bonding. A corner of the outer surface where the cutting operation starts is a portion where a stress is concentrated. Therefore, the corner of the outer surface on the substrate is vulnerable to crack even by a small impact. Cutting substrates by laser does not concentrate the stress on the corner of the substrate, which improves a resistance to impact.

After cutting the substrate completely, the liquid crystal is filled between the TFT substrate and the color filter substrate, at step ST**73**. Then, a liquid crystal introducing inlet is sealed at step ST**74**.

Next, polarizing plates are respectively attached to each outer surface of the TFT substrate and the color filter substrate, at step ST**75**.

After attaching the polarizing plates, the edges of the substrate is ground by laser, at step ST**76**. The grinding by laser prevents static charges from generated due to a friction on the substrate, which protects the thin film transistors formed on the inner surface of the TFT substrate from damages by the static charges.

After grinding, the liquid crystal display panel (hereinafter, referred to as LCD panel) is carried to an assembly line in order to be assembled with other element.

In the process of attaching the polarizing plate to the outer surface of the substrates according to the embodiment of the present invention, the polarizing plates are attached to each outer surface of the integrated substrates in a light transmitting type LCD panel, but the polarizing plate is attached to only one outer surface of the integrated substrate in a light reflecting type LCD panel.

On the other hand, in the above-described embodiment, after attaching the polarizing plate, the substrate is ground. However, the substrate can be ground before attaching the polarizing plate.

As shown in FIG. **8**, it is possible to perform the process of cutting the substrate along the cutting lines by using the laser light at step ST**82**, the process of filling the integrated substrates with the liquid crystal at step ST**83**, the process of sealing the liquid crystal introducing inlet at step ST**84**, the process of grinding the corner of the substrate at step ST**85**, and the process of attaching the polarizing plates to the substrates in sequence.

FIG. **9** is a sectional view of the cut surface **92** and the ground surface **94** of the substrate **90** which is cut according to the present invention. The surface **94** is ground to be round.

In the first embodiment of the present invention, both the cutting process and the grinding process are performed by laser. While the process of cutting the substrate is performed by using the laser light, however, by aligning laser focused on the outer surface of the substrate, of which an apsis is parallel and a minor axis is normal to the cutting line, the process of grinding the corner on the cut surface of the substrate can be omitted. Since the laser light with an ellipse shape round the edges of the cut surface, the grinding process is not required. In addition, the use of the laser light having the ellipse shape prevents the generation of glass chips on the inner surface of the substrate. Therefore, while connecting the end of a tape carrier package to the interconnection lines of the inner surface of the TFT substrate, the interconnection lines do not suffer from opening defect due to the glass chips.

According to the first embodiment, by eliminating glass chips that may generate during the cutting process, the defects in polarizing plate attachments and the short-cut problems of the interconnection lines while bonding the tape carrier package can be reduced. Further, since the laser grinding of the surface does not generate static charges, the thin film transistor can be safe from the damage by static charges.

Embodiment 2

The use of laser proposed in the first embodiment is effective for cutting the substrate. However, the use of laser according to the first embodiment is less effective for cutting the interconnection lines formed in the inner surface of the substrate. Therefore, it is required to provide a panel of which interconnection lines can be cut smoothly while cutting integrated substrates or single substrates.

FIG. **10** is a schematic plan view showing a relation of the interconnection lines **106** and the cutting lines **108** on the integrated substrate for the LCD panel according to the second embodiment of the present invention. In FIG. **10**, a reference numeral **104** denotes a black matrix having a square shape. The black matrix **104** is formed on one of the integrated substrates, for example on the color filter substrate, on which sealant is disposed to attach the substrates **102** together.

In FIG. **10**, the interconnection lines **106**, for example the data lines, adjacent to the cutting line **108** have ends spaced apart at a predetermined distance, for example about 1 mm, from the cutting line **108**. The interconnection lines, for example the gate lines, adjacent to the cutting line **109** also have ends spaced apart at a predetermined distance from the cutting lines **109**.

Accordingly, even if the integrated substrates **102** are cut by using the laser light or the diamond cutter along the cutting lines **108** and **109** thereon, cutting defects as shown in FIGS. **5**A and **5**B may not occur in the substrates **102** because the interconnection lines are not extended below the cutting lines.

In the second embodiment, on the other hand, when the thin film transistors are used to switch pixel electrodes, an insulating film or a passivation film is covered on one of the inner surfaces of the integrated substrates. If the insulating film and the passivation film extend across the cutting lines **108** and **109**, the insulating and passivation films can not be cut smoothly due to the property differences. Therefore, the insulating and passivation films must be formed within a region defined by the cutting lines **108** and **109** without extending below the cutting lines, in order to prevent the rough cut of those films.

The short bars **14** and **16** as shown in FIGS. **3** and **4** may be replaced with electrostatic diodes or protectors preventing the damage of static charges, which are formed within the region defined by the cutting lines **108** and **109**.

When testing the TFT panel, not a bundle of the interconnection lines but an individual interconnection line is tested by a probe.

FIG. **11** is a view showing the relation of the cutting line **122***a* and the liquid crystal introducing inlet **117** of the integrated substrate according to the another embodiment of the present invention. A reference numeral **114** denotes the black matrix formed on the inner surface of one of the integrated substrate. Reference numerals **118***a*, **118***b*, **122***a*, and **122***b* denote the cutting lines.

As shown in FIG. **11**, a sealing line for the liquid crystal introducing inlet **117** is positioned within the region defined by the cutting line **122***a*.

The relation of the liquid crystal inlet **116** and the cutting line **122***a* parallel to the liquid crystal inlet **117** will be described with reference to FIG. **13** below.

As shown FIG. **13**, the sealing line **116** near the liquid crystal introducing inlet **117** is formed in a square shape, which includes a first line **116***a* having an opening, a second line **116***b* extending vertically from an end of the first line **116***a* and having a first length, and a third line **116***c* extending from an end of the second line **116***b* to be parallel to the cutting line **122***a* and having a second length.

A distance between the third line **116***c* and the cutting line **122***a* preferably is about 1 mm.

Referring to FIGS. **12** and **13**, the sealing line **116** according to the embodiment of the present invention has the second line **116***b*. That is, a neck of the liquid crystal inlet is shorter than that of the structure according to the conventional art. Accordingly, the third line **116***c* extending parallel to the cutting line **122***a* remains after the cutting of the integrated substrate.

The third line **116***c* makes air to be introduced into the integrated substrates through a path between the sealing agent **126** and the third line **116***c* when the sealing agent **126** is sucked in the liquid crystal introducing inlet **117** to seal the liquid crystal introducing inlet **117** at the sealing process. Therefore, the path through which the air is introduced into the integrated substrates is longer than that of the conventional art, which substantially prevents the introduction of air.

The integrated substrates as constructed above are cut by emitting the laser light along the cutting line and spreading a refrigerant on the substrates to generate cracks.

Alternatively, the cutting lines are formed at a predetermined depth on the substrate using a diamond blade. Then, a small impact on the substrates along the cutting line may divide the substrates into a plurality of small-sized panels.

The substrate made of quartz can be used for the embodiment of the present invention. In this case, the panel according to the present invention can provide the same effect as the panel made of the glass substrate.

On the other hand, in the second embodiment of the present invention, the LCD panel is described as that the interconnection lines are positioned within the region defined by the cutting lines and that the sealing agent is disposed within the region defined by the cutting lines. However, both the interconnection lines and the liquid crystal introducing inlet may be located within the region defined by the cutting lines.

In the second embodiment as described above, since the interconnection lines, the corresponding electrodes, and the liquid crystal introducing inlet are positioned within the region of the substrate defined by the cutting lines, the interconnection lines are protected from rough cut during the cutting of the substrate.

Further, at the sealing process to enclose the liquid crystal introducing inlet, the introduction of the air into the liquid crystal layer is minimized to protect the liquid crystal layer.

Moreover, by introducing the laser cutting, the substrates can be cut under the same cutting condition, which simplifies the processes.

Embodiment 3

The LCD panel proposed in the second embodiment has the interconnection lines and the liquid crystal introducing inlet positioned within the region defined by the cutting lines, which requires the LCD panel design change. However, the LCD panel according to the third embodiment of the present invention can prevent an abnormal cutting of the interconnection lines without changing of the length of the interconnection lines.

FIG. **14** is a partially sectional view of the substrate to be cut according to the third embodiment of the present invention.

Referring to FIG. **14**, the glass substrate **32** is used as the substrate **142** to be cut, in which the conductive interconnection lines, for example the interconnection lines made from aluminum having a high toughness is arranged on the inner surface of the substrate **142** so that ends of the interconnection lines extend across the cutting lines. A reference character CL denotes the cutting line of the glass substrate. The substrate **142** is cut from the outer surface **142***b* to the conductive interconnection lines **146** through the inner surface **142***a* thereof.

A buffer layer **144** having a low toughness is disposed between the substrate **142** and the conductive interconnection lines **146**. The buffer layer **144** has a predetermined width along the cutting line CL. When the buffer layer **144** is cracked, the interconnection line **146** is also cracked together with the buffer layer **144**.

FIG. **15** is a perspective view of a color filter substrate to be cut according to still another embodiment of the present invention. FIG. **16** is a perspective view of a thin film transistor substrate to be cut according to still another embodiment of the present invention.

Referring to FIG. **15**, the color filter substrate **150** made from the glass substrate is provided as an object to be cut in which the color filter layer **154** having the red, green, and blue colors is formed on the inner surface **152***a* of the glass substrate **152**. The corresponding electrodes (not shown) are disposed on the color filter layer **154** of the color filter substrate **150**.

Since the corresponding electrodes lies along the cutting line **156**, the corresponding electrodes may not be cut precisely. Therefore, a buffer layer **158** of a predetermined width is disposed along the cutting line between the inner surface **152***a* of the substrate **152** and the corresponding electrodes.

The buffer layer **158** is made of metal having the low toughness as described above. Preferably, the buffer layer **158** is made of the same material as the black matrix layer (not shown) in the same process. In the third embodiment of the present invention, the black matrix layer and the buffer layer **158** are made of chromium (Cr).

Referring to FIG. **16**, the TFT substrate **160** containing the gate lines **164**, source lines **166**, pixel electrodes **168**, and thin film transistors **170** formed on the inner surface **162***a* of the glass substrate **162** is to be cut.

When the gate lines **164** and the source line **166** of the TFT **160** extend to the cutting line **174**, as described above, the abnormal cutting of the substrate may be performed. Therefore, the buffer layer **172** having the low toughness is disposed along the cutting line between extensions of the interconnection lines and the inner surface **162***a* of the glass substrate **162**.

The embodiment shown in FIGS. **14** to **16** can be cut using a laser cutter shown in FIG. **17**, without defects in cutting the interconnection lines.

Referring to FIG. **17**, the cutter is a device capable of cutting the substrate using the laser lights respectively having wavelengths w**1** and w**2**. The laser light having the wavelength w**1** (hereinafter, referred to as a first laser light) is used for generating the crack on the glass substrates **142**, **152**, and **162**, and the laser light having the wavelength w**2** (hereinafter, referred to as a second laser light) is used for generating the crack on the buffer layers **144**, **158**, and **172**.

A laser whose wavelength is 10.6 μm with an output of 50~250 w, such as a yag laser, CO_2 laser, gallium-arsenide laser and ruby laser can be used for those purposes.

The process of cutting the color filter substrate **150** and the TFT substrate **160** integrated together using the cutter of FIG. **17** will be described.

The integrated substrate is laid on a plate of the cutter **200**. The outer surface of the color filter substrate **150** is facing the cutter **200**.

A first laser light emitter **202** of the cutter **200** emits the first laser light having the wavelength w**1** focusing the cutting line **156** of the color filter substrate **150** and concentrating on the glass substrate **152**. A second laser light emitter **204** adjacent to the first laser light emitter **202** emits the second laser light having the wavelength w**2**, which in turn is transmitted through the glass substrate **152** and focused on the buffer layer **158**.

The glass substrate **152** and the buffer layer **158** are heated by the first and second laser light, which expand along the cutting line **156** in part and have the stress concentrated on the cutting line thereon.

A refrigerant spreading unit **206** following the second laser emitter **204** sprays a refrigerant at an interval of 0.1~0.3 second on the cutting line on which the stress is concentrated. Therefore, the glass substrate **152** and the buffer **158** which are heated by the laser lights are rapidly cooled.

The cutting lines of the glass substrate **152** and the buffer **158** are expanded and contracted by heat and refrigerant, so that the high stress is generated along the cutting lines.

When the stress is a larger than a combination force of glass molecules, the amorphous glass molecule structure is broken and the surface of the glass substrate **152** starts to crack.

At this time, a direction of the crack's creation and progression is the same as that of the laser radiation. That is, the crack is progressed from the outer surface to the inner surface of the glass substrate **152**, resulting in that the glass substrate **152** is cut thoroughly.

On the other hand, the buffer layer **158** has a stress thereon due to the expansion and contraction by the second laser light and the refrigerant applied on the buffer layer **158**.

When the stress is larger than a combination force of chromium atoms, a crystal structure of the buffer layer **158** is broken, resulting that a crack is created on the surface of the buffer layer **158**.

At this time, the crack is spread into the interconnection lines, which cut the corresponding electrodes on the edges of the interconnection lines smoothly along the cutting line of the glass substrate **152**.

As described above, after cutting the color filter substrate **150** completely, the integrated substrate is flipped over such that the outer surface of the TFT substrate is facing the laser cutter **200** and cut in such a manner as described above.

The color filter substrate **150** and the TFT substrate **160** used in the present embodiment are made of the same glass substrate and the same buffer layer. The first and second laser emitters for cutting the color filter substrate **150** can be used for cutting the TFT substrate without changing laser emitters.

On the other hand, the materials for the buffer layers of the color filter substrate and the TFT substrate may be different, depending on the material for the corresponding electrodes of the color filter substrate and the material for the interconnection lines of the TFT substrate. In such a case, when the color filter substrate is cut first and then the TFT substrate is cut, the buffer layer of the TFT substrate may not be smoothly cut. To solve this problem, the cutter shown in FIG. **17** may include another laser emitter capable of emitting a laser light having a third wavelength different from the first and second laser lights.

Regarding the above embodiment, while the substrate having a size corresponding to the panel size has been described, the laser cutter according to the present invention is suitable to cut the parent glass substrate having an area corresponding to a total area of at least two panels in order to improve the productivity.

In the above-described embodiment, although the laser cutter has been described to emit the first laser light so as to create the crack on the glass substrate and then to emit the second laser light so as to create the crack on the buffer layer, the laser cutter may emit the second laser light first and then the first laser light to cut the substrate.

According to the third embodiment of the present invention, when the LCD panel or the integrated glass substrate having the conductive interconnection lines thereon is cut by the laser cutter, by laying a buffer layer of low toughness and having a property of transferring the crack rapidly between the conductive interconnection lines and the glass substrate, the conductive interconnection lines can be smoothly cut.

While the present invention has been particularly shown and described with reference to a particular embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be effected therein without departing from the scope of the invention as defined by the appended claims.

What is claimed is:

1. A liquid crystal display panel, comprising:

a first substrate having wires form on a inner surface thereof, ends of the wires arranged near a cutting line of the first substrate;

a second substrate; and

sealant disposed between the first substrate and the second substrate, the sealant comprising:

a first portion disposed along edges of the first substrate, and second substrate and disconnected to form an inlet;

a second disposed extending outwardly from the first portion near the inlet; and

a third portion extending from the second portion.

2. The liquid crystal display of claim **1**, wherein each of the first substrate and the second substrate is a panel cut off from a parent glass substrate having an area larger than a sum of at least two panels.

3. The liquid crystal display of claim **1**, wherein the inlet is formed near the cutting line.

4. The liquid crystal display of claim **1**, wherein the inlet is formed near the cutting line.

5. The liquid crystal display of claim **4**, wherein the third portion of the sealant is spaced apart from the cutting line with a predetermined distance therebetween.

6. The liquid crystal display of claim **5**, wherein the predetermined distance is about 1 mm.

7. The liquid crystal display of claim **1**, wherein a distance between the ends of the wires and the cutting line is about 1 mm.

8. The liquid crystal display of claim **1**, further comprising:

an insulating layer formed on the wires; and

a passivation layer formed on the wires.

9. A substrate capable of being cut by a laser light, comprising:

a substrate having an outer surface with a cutting line and an inner surface;

a conducting layer deposited on the inner surface along a cutting line of the inner surface corresponding to the cutting line on the outer surface of the substrate;

sealant formed inside the cutting line; and

a buffer layer disposed along the cutting line between the inner surface and the conducting layer of the substrate,

wherein the substrate and the buffer layer are separately cut by laser lights having different wavelengths and the conducting layer is cracked by the buffer layer.

10. A liquid crystal display panel, comprising:

a first transparent insulating substrate including thin film transistors formed on an inner surface and a wire connected to the thin film transistors and pixel electrodes;

a second transparent insulating substrate having an inner surface corresponding to the first surface, a color filter formed on the inner surface, a black matrix and corresponding electrodes; and

a buffer layer disposed between the conducting layer and the inner surfaces and diffusing a crack generated therein to the conducting layer vertically,

wherein one of the first and second substrate has a cutting line on the outer surface thereof and the first and second substrates and the buffer layer are respectively cut by laser lights having a different wavelength, and

wherein a sealant is formed inside the cutting line.

11. The liquid crystal display panel of claim **10**, wherein the first substract and the second substrate are made of a parent glass substrate of an area larger than a sum of areas of at least two panels.

12. The liquid crystal display panel capable of claim **10**, wherein the buffer layer is formed with a predetermined width on the inner surface of one of the first and second substrates along a line corresponding to the cutting line formed on the outer surface of one of the first and second substrates.

13. The liquid crystal display panel of claim **10**, wherein the buffer layer is formed with a predetermined width on the inner surfaces of the first and second transparent insulating substrates along lines corresponding to the cutting line on the outer surface.

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